# SPONSORS

# Welcome to ESSDERC 2008

The European Solid-State Devices Research Conference (ESSDERC) and the European Solid-State Circuits Conference (ESSCIRC) are the premier events in the European research and development calendar. They have a long-established tradition of high-quality presentations covering major aspects of solid-state technology, devices, circuits and systems. Since 2002 the ESSCIRC and ESSDERC conferences have been organised jointly in recognition of the need for the two communities to interact in order to address the many challenges faced when designing highly complex systems in ever more advanced technologies and associated restrictions in design space.

This year the ESSDERC conference received 165 submissions originating from more than 20 countries, with 101 papers coming from Europe, 45 from Asia-Pacific and 16 from the Americas, demonstrating the international nature of ESSDERC. About 20% of the submissions came from industry, underlying the relevance of the conference. The difficult task of selecting the best papers was carried out by a 100-strong Technical Programme Committee (TPC) comprising world-class experts from academia, research institutes and industry. The TPC finally selected 71 papers for oral presentation. All papers received rigorous review with judgements made by more than 10 reviewers per paper.

The selected papers are organised in two parallel session tracks comprising three to five presentations. Both traditional and new topics are evident, namely advanced devices, IC manufacturing, telecommunication, high-voltage and power devices, modelling and simulation, characterisation and reliability, memory and system-on-chip technologies, sensors, MEMS, flexible electronics, bioelectronics, and emerging devices and nanotechnology. These regular sessions are combined with 12 invited papers for both ESSDERC and ESSCIRC. There are six invited speakers who will deliver joint plenary talks shared between the ESSDERC and ESSCIRC conferences, addressing topics of mutual interest, including flexible electronics, 3D integration and energy scavenging, together with perspectives on technology interfacing for fabless design companies, research for the 22 nm node and the

European position around “More Moore and More than Moore”. In addition, three speakers have been invited to address the ESSDERC community, focusing on topics relating to the future vision for devices and technology in the areas of memory, germanium, and III-V high-mobility channels and ultimate CMOS.

Three joint sessions have been organised to address topics of interest to both device and circuit communities. Two will tackle issues around process stability and yield in the light of the severe manufacturing variability associated with dopant statistics and linewidth definition, which are becoming evident as devices move to the atomistic scale. A third joint session will concentrate on components in high-frequency circuits.

The conference programme is complemented by a pre-conference day that is dedicated to tutorials aimed at both experienced and early-career research engineers and a post-conference day that includes several workshops.

We would like to thank all of the authors for their excellent contribution, which has made possible the high quality of the ESSDERC 2008 technical and scientific programme. We would also like to take this opportunity to acknowledge most warmly all of the members of the ESSDERC 2008 TPC for their hard work and dedication in their timely reviewing of all of the submitted papers and ensuring a high standard of technical and scientific quality. Particular thanks go to the conference secretariat for handling every aspect of this complex event with efficiency and competence, and for their tireless efforts and dedication.

We are looking forward to an exciting and high-level scientific programme, combined with many social activities that will give all delegates the opportunity to network and share experiences while enjoying the beautiful city of Edinburgh.

**Stephen Hall**
ESSDERC 2008
Technical Programme Committee chair

**Anthony Walton**
ESSDERC 2008
General chair

# About the IOP

The Institute of Physics is a scientific membership organisation devoted to increasing the understanding and application of physics. It has an extensive worldwide membership (currently around 35 000) and is a leading communicator of physics with all audiences, from specialists through government to the general public. Its publishing company, IOP Publishing, is a world leader in scientific publishing and the electronic dissemination of physics.

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ESSCIRC

For further information, visit **www.essderc2008.org**.

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# Timetable

## Tutorials

### Monday 15 September 2008

### CMOS at the Bleeding Edge
Harris Room (am)

| | |
|---|---|
| 08.30 | Introduction |
| 08.40 | **CMOS Scaling into the Next Decade: An Industrial Perspective of Challenges and Opportunities** |
| 09.20 | **High Mobility Channel MOSFET** |
| 10.00 | **Future Gate Stack Materials** |
| 10.40 | Coffee |
| 11.00 | **Variability** |
| 11.40 | **The SOI Mosfet: From Single Gate to Multigate** |
| 12.20 | Close |

### Characterisation for the Nanoelectronics Era
Ochill Room (pm)

| | |
|---|---|
| 13.45 | **Welcome and introduction tutorial session** |
| 14.00 | **Introducing Characterisation and Metrology** |
| 14.45 | **Physical Characterisation of High-K Materials** |
| 15.30 | Coffee break |
| 16.00 | **Two-Dimensional Carrier Profile Characterisation for Junction Engineering in Advanced Devices** |
| 16.30 | **Strain Measurements in Layers and Devices** |
| 17.15 | **Process Simulation for Advanced Stress and Junction Engineering** |
| 18.00 | Close |

## Integrating CMOS with other Technologies

Moorfoot Room (pm)

| | |
|---|---|
| 13.30 | **Introduction to Integrating CMOS with other Technologies** |
| 14.10 | **Design for Manufacture Challenges in MEMS Enabled Micro & Nano Systems** |
| 14.50 | **Post-Processing Microdisplays on CMOS** |
| 15.30 | Coffee break |
| 15.50 | **Post-Processing Image Sensors on CMOS** |
| 16.30 | **CMOS Integration with Biotechnology** |
| 17.10 | **Gas Multiplication Grid Integrated on CMOS** |
| 17.50 | Close |

## Tuesday 16 September 2008

| | |
|---|---|
| 08.50 | **Introduction** Pentland |
| 09.00–09.40 | **Joint plenary talk 1** R. Chau, Pentland |
| 09.50–10.50 | **Process Variability and Yield** Joint session, Pentland<br>**Reliability** Fintry<br>**High Voltage Devices** Sidlaw |
| 10.50–11.20 | Coffee break |
| 11.20–12.50 | **Channel Engineered Devices** Fintry<br>**Advanced Analogue Analogue Devices** Sidlaw |
| 12.50–14.10 | Lunch |
| 14.10–14.50 | **Joint plenary 2** V. Manian, Pentland |
| 15.00–15.40 | **ESSDERC plenary 1** T. Hamamoto, Fintry |
| 15.40–16.10 | **Coffee break and fringe session** Cromdale |
| 16.10–17.50 | **Floating-Gate and Charge-Trap Memories** Fintry<br>**Characterisation of Advanced Front-End Materials** Sidlaw |
| 18.30 | **Welcome reception, including whisky tasting**<br>Cromdale Hall |

ESSDERC ESSCIRC 2008

## Wednesday 17 September 2008

08.30–09.10 **Joint plenary 3** C. Van Hoof, Pentland

09.30–10.10 **ESSDERC plenary 2** D. Antoniadis, Fintry

10.10–10.40 Coffee break

10.40–12.20 **SRAM and Alternative NV Memories** Fintry

**Applied Modelling Techniques** Sidlaw

12.20–13.50 Lunch

13.50–14.30 **Joint plenary 4** T. Sakurai, Pentland

14.40–16.00 **Process Stability** Joint session, Pentland

**Fully Depleted Devices** Fintry

**Carbon Nanotubes and New Materials** Sidlaw

16.00–16.30 Coffee break

16.30–17.50 **Characterisation of Advanced Devices** Fintry
**Progress in Device Modelling** Sidlaw

19.00 **Conference dinner** Murrayfield Stadium

## Thursday 18 September 2008

08.30–09.10 **Joint plenary 5** M. Thompson, Pentland

09.30–10.50 **Optical Detectors** Fintry
**Transistor Engineering** Sidlaw

10.50–11.20 Coffee break

11.20–12.40 **Sensors and MEMS** Fintry
**Emerging Silicon Devices** Sidlaw

12.40–14.10 Lunch

14.10–14.50 **Joint plenary 6** V. Subramanian, Pentland

15.00–15.40 **ESSDERC plenary 3** T. Krishnamohan, Fintry

15.40–16.10 Coffee break

16.10–17.50 **Source and Drain Engineering** Fintry

# General information

**General organisation**
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Tel +44 (0)131 560 5624
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| | |
|---|---|
| **Conference chair** | Anthony Walton, University of Edinburgh |
| **Deputy chair** | Peter Ashburn, University of Southampton |
| | |
| **ESSDERC TPC chair** | Steve Hall, University of Liverpool |
| **Deputy chair** | Asen Asenov, University of Glasgow |
| **Vice-chair** | A Dimoulas, IMEL/NCSR Demokritos |
| | |
| **Tutorial chairs** | |
| **ESSDERC** | Anthony O'Neil, Newcastle University |
| **Workshop chair** | Anthony O'Neil, Newcastle University |
| **ESS-fringe poster chairs** | A J Snell, University of Edinburgh |
| | J T M Stevenson, University of Edinburgh |
| **Local chair** | Les Haworth, University of Edinburgh |
| | |
| **Local organising committee** | |
| Scott Roy | University of Glasgow |
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| Tom Stevenson | University of Edinburgh |
| Stewart Smith | University of Edinburgh |
| Jon Terry | University of Edinburgh |
| | |
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| Ralf Brederlow | Texas Instruments |
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| Christian Enz | CSEM |
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| Jürgen Lorenz, FhG | IISB |

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| Bernd Meinerzhagen | TU Braunschweig |
| Robert Mertens | IMEC |
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| Hideki Oka | Fujitsu Labs |
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# Welcome to Edinburgh

Edinburgh is located in the south-east of Scotland. It has been the capital of Scotland since 1437 and is the seat of the Scottish Parliament. Owing to its rugged setting and vast collection of medieval and Georgian architecture, including numerous stone tenements, it is often considered to be one of the most picturesque cities in Europe. The Old Town and New Town districts of Edinburgh were listed as a UNESCO World Heritage Site in 1995.

The city is well known for the annual Edinburgh Festival – a collection of official and independent festivals held annually over about four weeks starting in early August. Edinburgh is one of Europe's major tourist destinations, attracting around 13 million visitors a year, and it is the second most visited tourist destination in the UK, after London.

**Climate**

The climate in Edinburgh is relatively mild in September. However, the weather can change quickly throughout the day – a rainy morning can often be followed by a sunny afternoon. It is therefore advisable to come prepared for a mild but rainy climate.

**Time zone**

Western Europe daylight/summertime (GMT + 1:00)

**Electricity**

Requires UK standard three-pin plug, 220–240 V, 50 Hz.

**Currency**

The Scottish currency is the British Pound Sterling. Bank of England banknotes are accepted as legal currency, in addition to those

issued by the Bank of Scotland, the Royal Bank of Scotland and the Clydesdale Bank. Some retail outlets and visitor attractions will also accept Euros.

**Tips**

It is customary to pay 10% in a restaurant or café, although this is only expected if there is waiter service. If it is a takeaway or self-service establishment you will not be expected to tip.

**Banks**

Most banks are usually open Monday to Friday from 09.30 to 16.00/17.00. Some larger branches may also be open later on Thursdays and on Saturday mornings. Avoid changing money or cheques in hotels because the rates are usually very poor.

**Emergency calls**

In case of emergency, dial 999 for the police or fire services.

**Passport and visa**

Visitors from some countries require a visa to enter the UK. Please check with your travel agent. Participants who require a visa should allow plenty of time for their application to be processed. The Institute of Physics can issue the standard letter of invitation to those participants with an accepted presentation at the conference and from whom payment has been received in full for their registration. For those not making a presentation, the Institute of Physics cannot issue invitation letters. Delegates will instead receive a letter confirming the conference details and confirmation of payment of registration.

**Hotels**

To arrange accommodation while at the conference, please contact BSI, quoting “IOP” (tel 0870 830 4266; e-mail IOP@bsi.co.uk). Information about all hotels can be found in the “Hotels” section of

the websites at **www.essderc2008.org** and **www.esscirc2008.org**.

More information about the city is available on the Edinburgh Tourist Board website at **www.edinburgh.org**.

# Conference site

The conference, tutorials, workshops and exhibition will be held at:

**Edinburgh International Conference Centre** (EICC)
The Exchange
Edinburgh EH3 8EE
Tel 0131 300 3000
**www.eicc.co.uk**

**How to get to there**
The Edinburgh International Conference is located at the heart of Scotland's capital city. Its prime central location ensures easy access via road, rail and air, and many of its famous and historical attractions are within walking distance. A range of hotels to suit all budgets and requirements are also within a short distance of the centre.

The EICC is arranged over four levels and part of its attraction is the versatility and space available. On arriving in the conference centre, you will find yourself in the Strathblane Hall, where you will be able to register for the conference.

**By plane**
For the latest information about flights to Edinburgh, visit the website at www.edinburghairport.com. There are a number of ways to travel into the city centre from the airport, as described below.

**By taxi**
There is an excellent taxi service direct from the airport to the city. You'll find official airport taxis at the taxi rank outside the terminal building (follow the signs inside the airport). It costs about £15 to get a taxi from the airport to the city centre and the journey takes around 20 minutes, depending on traffic flow and time of day.

**Local taxi numbers**
**Computer Cabs**
Tel 0131 272 8000
**www.comcab-edinburgh.co.uk**

**Festival City Cars**
Tel 0131 552 1777
**www.festivalcitycars.co.uk**

**CITY CENTRE MAP**

The Exchange, Morrison Street,
Edinburgh EH3 8EE.
T: 0131 300 3000 F: 0131 300 3030
W: www.eicc.co.uk E: sales@eicc.co.uk

The main entrance to the EICC is on **Morrison Street** where there is a coach drop off point.

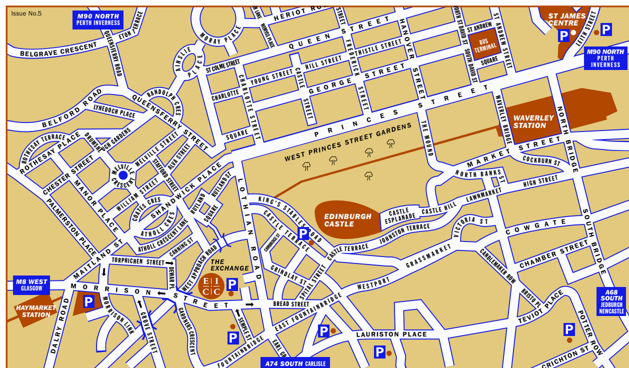
Access to the EICC Loading Bay is from the **West Approach Road**.

There are a number of car parks within walking distance of the EICC, they are marked on the map. For further details on car parking please visit our website.

Please note that there are a number of one way streets in close proximity to the EICC.

After 18.30 street parking is allowed in certain areas.

Please be advised that these maps cannot be reproduced without the permission of Ordnance Survey.

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## By coach

The Airlink 100 operates a frequent bus service (every 10 minutes at peak times) between Edinburgh Airport and the city centre, with designated stops *en route*. Regular bus services start at 04.45 and run until 00.22 at night. The journey time is 20 minutes, with tickets costing £3.00 single and £5.00 return. Delegates are advised to disembark at Haymarket Railway Station and to follow signs for the EICC on foot (a five-minute walk). Also, the N22 bus departs from stand 19 and runs every 30 minutes through the night until the Airlink service starts again. For more information about these services, visit www.flybybus.com.

## By Edinburgh Shuttle

The Edinburgh Shuttle is a door-to-door shared transport service between Edinburgh Airport and the city centre. Fares start at £8.00 for an individual with reduced rates for passengers travelling together to the same destination. Visit **www.edinburghshuttle.com** or tel 0845 500 5000.

## Arriving by train

Edinburgh has two railway stations: Waverley and Haymarket. Waverley is the main station and has direct routes to many cities across the country. For more information, visit www.nationalrail.co.uk. Haymarket is just a five-minute walk from the EICC. Waverley is a few minutes away by taxi.

## By bus

Edinburgh's main bus terminal is located at St Andrew's Square. Bus connections stretch right across the UK. For details of these routes, visit www.nationalexpress.com or www.citylink.co.uk.

**By car**

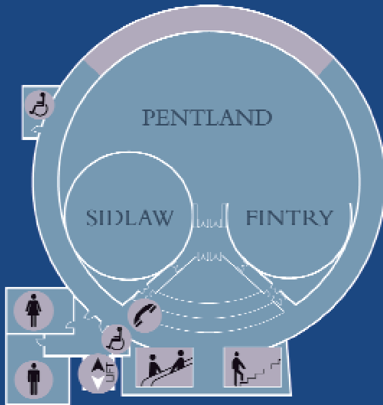
The EICC is right in the centre of Edinburgh. The main entrance is on Morrison Street. For directions from your home or office, visit www.theaa.com and input EH3 8EE for the destination postcode into the route planner.

**Local buses**

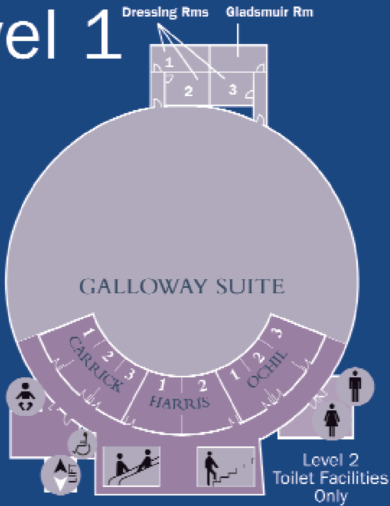
Numbers 2 and 12 depart approximately 200 yards from the entrance to the EICC on Morrison Street and run every 15 minutes between 07.00 and 23.30. There are regular city bus services to Lothian Road and Shandwick Place. Delegates should follow directional signage from Lothian Road and Shandwick Place to the EICC. Buses require the exact change: £1.10 for any journey; day tickets are available for £2.30. For further information, visit the Lothian Buses website at **www.lothianbuses.co.uk**.

# Conference venue

## Level 3

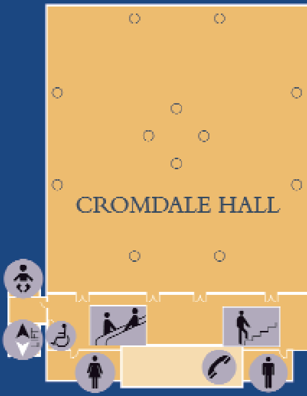



## Level 1



# Level 0

# Level -2




Level -1
Telephone Facilities Only

# Conference facilities

**Car parks**
There are a number of car parks, all within five minutes' walking distance from the EICC. Local car parks are highlighted on the EICC city centre map (p16).

**Morrison Street car park**
Capacity: 400 spaces.
Approximate rates: £1.00 (hourly rate)/£5.00 (4–6 h)/£7.20 (8 h)/£2.50 (from 17.00 until 07.00).
Contact: enquire at the registration desk or tel 0131 477 7000

**Semple Street (Thistle Parking)**
Capacity: 200 spaces.
Approximate rates: £1.00 (up to 6 h)/£8.00 (6–10 h)/£10.00 (more than 10 h)
Contact: tel 0131 225 7480

**EICC Morrison Street**
Capacity: 88 spaces
Approximate rates: £1.00 (up to 1 h)/£5.00 (4–6 h)/£7.20 (more than 8 h)/£2.50 (from 17.00 until 07.00)
Contact: enquire at the registration desk or tel 0131 477 7000

**Castle Terrace**
Capacity: 750 spaces
Open 24 hours
Approximate rates: £2.50 (up to 2 h)/£7.00 (4–6 h)/£10.50 (9–24 h)/£3.00 (from 17.00 until 06.00)
Contact: tel 0131 229 2870

**Public phones**
For outgoing calls, coin/card-operated phones are available in the Business and Media Centre on Level 0 and near the main escalator/stairs on Levels 2 and 3.

**Cloakroom and toilets**
Cloakroom facilities can be found next to the lifts in the Strathblane Hall on Level 0. Toilets can be found on every level of the conference centre next to the main escalators/stairs.

**Left luggage**
A left luggage area will be available at the cloakroom in the Strathblane Hall, particularly during peak times for delegate arrival

and departures. Please visit the registration desks near the cloakroom if you have any special requirements.

**Drink and food facilities**
There are coffee/tea machines throughout the venue, all of which accept cash. There is also an area in the Strathblane Hall selling soft drinks and light snacks.

**Disabled access**
Please contact the registration desk or make yourself known to a member of EICC staff, who will assist with any access or facility requirements.

**Fire and evacuation procedures**
Fire exits are located in each of the four corners of the building and are well signposted. In the unlikely event of an emergency, please leave the building in an orderly manner, as directed. Do not use the main stairs or escalators. On exiting the building, we will ask you to move to muster points as advised by the stewards and emergency marshals.

# Conference registration

**Conference registration desk**
The registration desk will be situated in the Strathblane Hall and will be open throughout the conference at the following times:

| | |
|---|---|
| **Sunday** | 16.00–19.00 |
| **Monday** | 08.00–18.30 |
| **Tuesday** | 08.00–18.30 |
| **Wednesday** | 08.00–18.30 |
| **Thursday** | 08.00–18.30 |
| **Friday** | 08.00–18.00 |

On arrival, all participants will be given a registration pack containing conference material and a lapel badge, which must be worn at all times during the conference. Replacement badges can be issued at the registration desk.

To contact the ESSDERC-ESSCIRC registration desk, tel +44 (0)131 519 4123.

**Messages**
There will be a message board next to the registration desks in the Strathblane Hall. All messages must be given to a member of the conference team, who will then be able to post them on the board. Plasma screens throughout the EICC will broadcast up-to-date information about the technical programme.

# Conference information

**Internet access**
Wireless internet access will be available throughout the EICC. This will be free of charge during the conference and exhibition, and passes can be collected from the registration desk throughout the event. For one-off access to a PC and the internet, there will be several computers in the Business and Media Centre, charged at an hourly rate.

**Official language**
The congress language is English.

**Speakers briefing**
Authors should meet their chairperson in the session room 20 minutes prior to the beginning of their respective sessions.

**Conference proceedings**
All participants will receive a copy of either the ESSDERC or the ESSCIRC Proceedings and a USB device containing the accepted papers for both.

**Best Paper Award**
ESSDERC/ESSCIRC offers a Best Paper Award (for contributed papers only) and a Young Scientist Award for the best paper presented by a speaker under the age of 28. Selection is based on evaluation by the audience and paper ratings.

**Insurance disclaimer**
Participants are responsible for their own insurance. The Institute of Physics, Trinity College and their approved representatives cannot take responsibility for any accident, loss or damage to participant or their property during the event.

**Complaints**
While we hope that your time at the conference is enjoyable, if you encounter a problem during your stay, please report it to the registration desk as soon as possible. The conference team will make every effort to rectify the issue.

# Conference overview

### Sunday 14 September 2008

| | |
|---|---|
| Registration | Strathblane Hall |

### Monday 15 September 2008

| | |
|---|---|
| Registration | Strathblane Hall |
| Tutorials | Harris 1, Moorfoot Suite, Kilsyth Suite, Tinto Suite |
| Buffet lunch | Strathblane Hall |
| Fringe | Cromdale Hall |

### Tuesday 16 September 2008

| | |
|---|---|
| Registration | Strathblane Hall |
| Conference opening | Pentland Suite |
| Technical sessions | Pentland Suite, Sidlaw Suite, Fintry Suite, Carrick Suite, Harris 1, Ochil Suite, Tinto Suite, Moorfoot Suite, Kilsyth Suite |
| Buffet lunch | Cromdale Hall |
| Exhibition | Cromdale Hall |
| Fringe | Cromdale Hall |
| Welcome reception | Cromdale Hall |
| Women’s event | University of Edinburgh |

### Wednesday 17 September 2008

| | |
|---|---|
| Registration | Strathblane Hall |
| Technical sessions | Pentland Suite, Sidlaw Suite, Fintry Suite, Carrick Suite, Harris 1, Ochil Suite, Tinto Suite, Moorfoot Suite, Kilsyth Suite |
| Buffet lunch | Cromdale Hall |
| Exhibition | Cromdale Hall |
| Fringe | Cromdale Hall |
| Conference dinner | Murrayfield Stadium |

### Thursday 18 September 2008

| | |
|---|---|
| Registration | Strathblane Hall |
| Technical sessions | Pentland Suite, Sidlaw Suite, Fintry Suite, Carrick Suite, Harris 1, Ochil Suite, Tinto Suite, Moorfoot Suite, Kilsyth Suite |
| Buffet lunch | Cromdale Hall |
| Exhibition | Cromdale Hall |
| Fringe | Cromdale Hall |

**Friday 19 September 2008**

| | |
|---|---|
| Registration | Strathblane Hall |
| Workshops | Sidlaw Suite, Carrick Suite, Harris 1, Harris 1, Ochill Suite, Tinto Suite, Moorfoot Suite, Kilsyth Suite |
| Buffet lunch | Stathblane Hall |

# Meals and refreshments

All meals and refreshments will be served at allocated times during the conference programme.

### Monday 15 September 2008

| | |
|---|---|
| Morning refreshments | Strathblane Hall |
| Buffet lunch | Strathblane Hall |
| Afternoon refreshments | Strathblane Hall |

### Tuesday 16 September 2008

| | |
|---|---|
| Morning refreshments | Cromdale Hall |
| Buffet lunch | Cromdale Hall |
| Afternoon refreshments | Cromdale Hall |
| Welcome reception | Cromdale Hall |

### Wednesday 17 September 2008

| | |
|---|---|
| Morning refreshments | Cromdale Hall |
| Buffet lunch | Cromdale Hall |
| Afternoon refreshments | Cromdale Hall |
| Conference dinner* | Murrayfield Stadium |

### Thursday 18 September 2008

| | |
|---|---|
| Morning refreshments | Cromdale Hall |
| Buffet lunch | Cromdale Hall |
| Afternoon refreshments | Cromdale Hall |

### Friday 19 September 2008

| | |
|---|---|
| Morning refreshments | Strathblane Hall |
| Buffet lunch | Strathblane Hall |
| Afternoon refreshments | Strathblane Hall |

*The conference dinner is inclusive in the conference fee and must be prebooked. To reserve additional places, email faye.heran@iop.org in advance.

# Social programme

### Tuesday 16 September

**Welcome reception**

A welcome reception will take place from 18.30 to 20.30 in the Cromdale Hall. This will include a whisky-tasting session, offering delegates the opportunity to sample traditional whiskies and cheeses from across Scotland. Wine and soft drinks will also be available.

### Tuesday 16 September

**Women's event and dinner**

This will take place in the evening. For further details, please enquire at the registration desk during the conference or refer to the websites at www.essderc2008.org or www.esscirc2008.org.

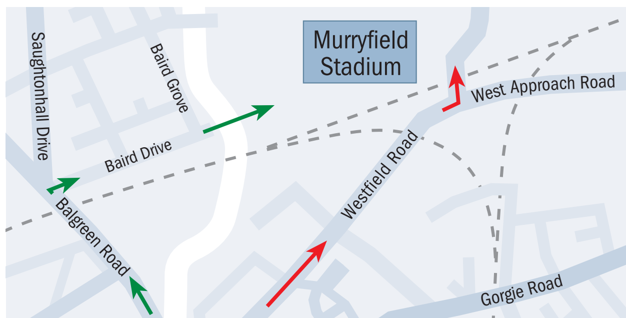
### Wednesday 17 September

**Conference dinner**

The conference dinner will be held at Murrayfield Stadium, the home of Scottish Rugby, from 19.00 to 01.00. It will consist of a three-course Scottish-themed menu in the Thistle and Presidential Suite and will be preceded by a Pitchside drinks reception (weather permitting) with traditional Scottish entertainment. Coaches will be provided to transport participants to and from the EICC.

Participants with special dietary requirements are asked to notify the conference organiser prior to their arrival. Unfortunately it will not be possible to provide an alternative menu unless prior notification has been received.

For further information about Murrayfield Stadium, visit the website at www.murrayfieldexperience.com




**Travelling to the Murrayfield Stadium**

**Shuttle service**

Coaches will be scheduled to take all delegates to and from Murrayfield Stadium at the following times:.

**EICC to Murrayfield Stadium**

There will be three pick-ups from the front of the EICC at 18.30, 19.00 and 19.30.

**Murrayfield Stadium to EICC**

A shuttle service will run between 22.30 and 24.00, picking up outside Murrayfield Stadium and dropping off outside the EICC and Princess Street. For all delegates returning after 24.00, it is advised that a private taxi is booked beforehand. Taxi numbers are provided on p15.

**Independent travel**

For those who wish to arrange independent travel to and from Murrayfield Stadium, details of the location and directions to the venue are provided below:

**Murrayfield Experience**
Edinburgh
Midlothian EH12 5PJ
Tel 0131 346 5250
E-mail enquiries@murrayfieldexperience.com

Murrayfield Stadium is situated in West Edinburgh, six miles from the International Airport, three miles from Edinburgh Waverley Railway Station, one mile from Haymarket Railway Station and close to the city bypass, and the M8 and M9 motorways.
A map of the location is provided below. Please note that the green arrows are for match-day routes and the red arrows are normal business days.

# Accompanying persons programme

As a world-class tourist destination, the Edinburgh naturally offers a multitude of activities, whatever time of year you visit. Located within easy walking distance of the EICC, Edinburgh's Old Town is a fascinating district of cobbled streets, alleys and courtyards. The Royal Mile is a clear favourite with visitors, offering a variety of museums, shops and, of course, the world-famous Edinburgh Castle. Ghost tours take place every evening around the Old Town, alluding to perhaps the more sinister side of Edinburgh's past. Open-top bus tours are an excellent way of viewing the whole city. Linking the Old Town with the Royal Yacht Britannia, these explore Edinburgh's Georgian New Town and Holyrood Park. Simply hop on and off the bus to visit your favourite attractions.

A list of attractions can be found on the Edinburgh Tourist Board website at **www.edinburgh.org**. Some that we particularly recommend are listed below.

**Dynamic Earth**
Based in the heart of Edinburgh, Dynamic Earth tells the story of our planet's past, present and future.
Price per person: adult £9.50/child £5.95 (3–15 years)
Opening times: 10.00–18.00
**www.dynamicearth.co.uk**

**Edinburgh Castle**
The castle is the best known and most visited of historic buildings in the city. Perched on an extinct volcano and offering stunning views, this instantly recognisable fortress is a powerful national symbol and part of Edinburgh's world heritage site.
Price per person: adult £12.00/Child £6.00 (5–15 years)
Opening times: 09.30–18.00
**www.edinburghcastle.gov.uk**

**Museum of Edinburgh**
The Museum of Edinburgh, formerly known as Huntly House, occupies a series of picturesque 16th- and 17th-century buildings in the heart of the Old Town. It illustrates the history of the city from the earliest settlement to the present day.
Admission free
Opening times: 10.00–17.00 (Monday to Saturday)
**www.cac.org.uk**

**National Museums Scotland**
This family of attractions includes the National Museum of Scotland, the National War Museum, the National Museum of Costume, the National Museum of Rural Life, the National Museum of Flight and the National Museums Collection Centre.
Price per person: varies from free admission to £8.50
Opening times: 10.00–17.00
**www.nms.ac.uk**

**The Palace of Holyroodhouse**
Founded as a monastery in 1128, the palace is The Queen's official residence in Scotland. Situated at the end of the Royal Mile, the it is closely associated with Scotland's turbulent past, including

Mary, Queen of Scots, who lived here between 1561 and 1567. Successive kings and queens have made the Palace of Holyroodhouse the premier royal residence in Scotland.
Price per person: adult £9.80/child £5.80 (5–17 years)/free (under 5 years)
Opening times: 09.30–18.00 (last admission 17:00)
**www.royal.gov.uk**

**Edinburgh Zoo**
The largest and most exciting wildlife attraction in Scotland, the zoo is committed to the highest standards of animal welfare, conservation and environmental education.
Price per person: adult £11.50/child £8.00 (3–14 years)/free (under 3 years)
Opening times: 09.00–18.00
**www.edinburghzoo.org.uk**

**Time Out guide**
*Time Out* provides an up-to-date guide to accommodation and attractions, a current events calender and restaurant reviews. The guide for Edinburgh can be found online at
**www.timeout.com/travel/edinburgh.**

**Edinburgh pass**
The Edinburgh pass offers free travel, plus discounts on shopping, meals and visitor attractions around the city, together with a comprehensive guidebook. Passes range from one to three days and can be purchased online at **www.edinburgh.org/pass**, which also offers maps, information about the city and suggested itineries for a short visit.

# Exhibition

**Hosted by JEMI UK**
**www.jemiuk.com**

The exhibition is a new addition to the ESSSDERC/ESSCIRC format and will include representation from a number of equipment and materials suppliers as well as major scientific publishers. It will take place in the Cromdale Hall on Level 2 and will run from Tuesday 16 To Thursday 18 September. All refreshment and lunch breaks will be hosted in the exhibition area during the main conference days, together with the welcome reception on Tuesday 16 September and the fringe sessions.

A separate exhibition handbook will be produced and can be collected from the registration desk on arrival.

**Opening hours**

| | |
|---|---|
| Tuesday 16 September | 08:00–18:00 |
| Wednesday 17 September | 08:00–18:00 |
| Thursday 18 September | 08:00–18:00 |

**Exhibition organisers**

Ingrid Prince
Business manager
JEMI UK Ltd
Tel +44 (0)131 650 7815
Fax +44 (0)131 650 7475
E-mail jemi-enquiries@see.ed.ac.uk

# Joint plenary talks

## Emerging Device Nanotechnology for Future High-Speed and Energy-Efficient VLSI: Challenges and Opportunities

Chau, Robert
Intel Corporation

Emerging device nanotechnologies as well as their integration on large silicon wafers present both challenges and opportunities for future high-speed and energy-efficient digital VLSI applications.
a
**Robert Chau** received a BSc, an MS and a PhD in electrical engineering from Ohio State University, Columbus, Ohio. He is an Intel senior fellow and director of transistor research and nanotechnology at Intel Corporation, Hillsboro, Oregon, and is responsible for directing R&D in advanced transistors and gate dielectrics, process modules and technologies, and integrated processes for microprocessor applications. He has developed seven generations of Intel gate dielectrics, along with many transistor innovations used in various Intel logic processes, since joining Intel in 1989. He is also responsible for leading research efforts in emerging nanotechnologies for future nanoelectronics applications. He holds more than 75 US patents and has received six Intel Achievement Awards and 13 Intel Logic Technology Development Division Recognition Awards. He was recognised by *Industry Week* in 2003 as one of the 16 "R&D Stars" in the US who "continue to push the boundaries of technical and scientific achievement".

Founded in 1968, Intel Corporation is the world's largest semiconductor company and has recently demonstrated a functional 32 nm logic process SRAM with 1.9 B second-generation high-k metal gate transistors.

## Technology Interfacing for Fabless Semiconductor Companies

Manian, Vahid
Broadcom

Today the semiconductor industry faces unprecedented challenges, and those companies that meet these challenges through collaboration, integration and innovation will be the winners of huge new market opportunities from mobile convergence to emerging biomedical markets. The semiconductor industry has matured and consequently overall revenue growth rates have fallen to single digits, while the number of units continues to grow robustly. Volume and pricing are on opposite trajectories. The triangulation of increasing volumes; decreasing ASPs; and higher R&D investment just to stay in the game is putting serious profitability pressure on companies. The design of new products is accelerating in terms of both costs and complexity. Today it costs a minimum of $15–$30m to reach tape-out, and there doesn't seem to be an end in sight. Companies currently allocate 17% of their revenue to R&D, and this is expected to be 20% by 2012. There are many factors behind this acceleration, including the exponentially growing role of process technology development and software design. Most leading-edge companies now have more software design engineers than hardware engineers.

As the cost of developing new process technology increases and building new fabrication facilities grows exponentially, more and more traditional large semiconductor companies and traditional integrated design manufacturers are

migrating to either a fabless model or a fab-light strategy. The fabless business model has clearly won and nearly all companies outside microprocessors and memory have adopted it. And, despite the reliance on foundries, there are some challenges that both large and small semiconductor companies face.

Some of the questions facing today's fabless semiconductor companies are:

- Do we still need specific technology knowledge to support SOC development?
- How much detail do you need in the process technology nodes?
- How do we deal with modelling issues?
- What is provided from a foundry versus what a company needs?
- How do you deal with yield improvement and cost reduction?

Broadcom is one of the early adopters of this business model and has grown from zero to a nearly $4bn semiconductor company by adhering to this model and navigating through these challenges. We still believe that this is the successful model for the future and need to continue our investment in partnership with the critical elements of our supply chain

**Vahid Manian** is the senior vice-president of global manufacturing operations for Broadcom Corporation. In this position he is responsible for all manufacturing activities, including foundry operations and process technology direction. Manian joined Broadcom in January 1996 as director of operations and became vice-president of manufacturing operations in December 1997. Previously, he served in a number of positions for approximately 12 years at Silicon Systems Inc, a semiconductor manufacturer, including more than six years as director of operations. At Silicon Systems he led the implementation, production ramp and qualification of advanced PRML-read channel integrated circuits. He received a BSEE and an MBA from the University of California, Irvine.

## Micropower Energy Scavenging

van Hoof, Chris
IMEC

More than a decade of research in the field of thermal, motion and vibrational energy scavenging has resulted in increasing power output and smaller embodiments. Power-management circuits for rectification and DC–DC conversion are becoming able to convert the power from these energy scavengers efficiently. This paper summarises recent energy-scavenging results and their power-management circuits.

**Chris Van Hoof** received a PhD in electrical engineering from the University of Leuven, Belgium, in collaboration with IMEC in 1992. He is currently director of the Integrated Systems Department of the Microsystems, Components and Packaging Division at IMEC, Leuven, Belgium. At IMEC he became successively head of the detector systems group in 1998, director of the Microsystems Department in 2002 and director of the Integrated Systems Department in 2004. His research concerns several key ingredients of autonomous sensor nodes (sensor front-ends, energy scavenging) and is largely focused on advanced packaging and interconnect technology (2D and 3D integration, RF integration). Van Hoof has contributed to two cornerstone ESA flight missions. Since 2000 he has also been a guest professor at the University of Leuven, and he is currently the promoter of eight doctoral theses. He has written more than 130 publications and given 20 invited talks.

The Interuniversity Microelectronics Centre (IMEC) is a research facility based in Leuven, with affiliated laboratories throughout Flanders. Its approximately 1500 employees focus on next-generation electronics, 3–10 years ahead of industry needs.

## Solving Issues of Integrated Circuits by 3D-Stacking Meeting with the Era of Power, Integrity Attackers and NRE Explosion and a Bit of Future

Sakurai, Takayasu
University of Tokyo

In the foreseeable future, VLSI design will meet a few explosions: an explosion of power and an explosion of integrity attackers, including power integrity and signal integrity, and an explosion of non-recurring engineering cost (NRE). A remedy for the power explosion and the explosion of integrity attackers lies in "voltage engineering". A remedy for the NRE explosion is to reduce the number of developments and sell tens of millions of chips with a fixed design. A 3D-stacked LSI approach may embody such a possibility.

**Takayasu Sakuri** received his PhD in electrical engineering from the University of Tokyo, Japan, in 1981. That year he was with Toshiba Corporation, where he designed CMOS DRAM, SRAM, RISC processors, DSPs and SoC Solutions. He has worked extensively on interconnect-delay and capacitance modelling, known as the Sakurai model, and an alpha power-law MOS model. From 1988 to 1990 he was a visiting researcher with the University of California, Berkeley, where he conducted research in the field of VLSI computer-aided design. Since 1996 he has been a professor with the University of Tokyo, working on low-power, high-speed VLSI; memory design; interconnects; and wireless systems. Sakuri has published more than 400 technical papers (including 70 invited) and several books, and he has filed more than 100 patents. He is a consultant to a number of US start-ups. He served as a conference chair for the symposium on VLSI Circuits and ICICDT, a vice-chair for ASPDAC, a TPC chair for the first A-SSCC and VLSI symposium, and a programme committee member for IEEE ISSCC, CICC, DAC, ESSCIRC, ICCAD, ISLPED and other international conferences. Sakuri was a plenary speaker for the 2003 ISSC. He is an elected AdCom member for the IEEE Solid-State Circuits Society and a Distinguished Lecturer of the IEEE Circuits and Systems Society. He was a recipient of the 2005 IEEE ICICDT Award, the 2005 IEEE ISSCC Takuo Sugano Award and the 2005 P&I Patent of the Year Award.

## More Than Moore and More Moore in Europe

Michael Thompson
STMicroelectronics

A brief summary of the trends over the last 10 years for design and manufacturing activity in Europe is presented, covering the More Moore and More than Moore technologies. Some of the difficulties in maintaining the traditional paradigm are then presented, covering the barriers to (re-)entry in the More Moore field as well as some methods to address them. The same presentation for the More than Moore field is then made. From this, a number of conclusions are drawn, including the important role that Europe has to play in shaping design, technology and manufacturing going forward.

**Michael Thompson** graduated from the University of Glasgow, UK, with a degree in astronomy with advanced mathematics. He started working in 1980 at General Instrument Microelectronics, Glenrothes, as a photolithography

engineer, then joined Inmos at Newport, a 100 mm fab specialising in high-performance memories and microprocessors, which was acquired in 1989 to become part of SGS-THOMSON, where he worked as process development manager and engineering manager. In 1991 Thompson moved to ST Microelectronics, Crolles, ST's first 200 mm fab, where he was appointed operations director. He was involved in the first process technology development collaboration between ST Microelectronics and Philips from its start in 1992, as well as in the creation of the ST Microelectronics–France Telecom-CEA/Leti Centre Commun. By 2005 he had the double responsibility of managing the 200 mm fab and contributing to the start-up of Crolles 2, the new 300 mm state-of-the-art facility, specialising in high-performance technologies for system on chip. He is currently group VP of front-end technology and manufacturing, advanced R&D – high-performance logic and derivatives.

ST Microelectronics (originally SGS-THOMSON) was formed in 1987 from long-established semiconductor companies SGS Microelettronica and Thomson Semiconducteurs, It has approximately 50 000 employees, together with 16 R&D units and 39 design and application units in front-end technology and manufacturing.

### Printed Electronics for Low-Cost Electronic Systems: Technology Status and Application Development

Subramanian, Vivek
University of California, Berkeley

Recently, printing has received interest for realising low-cost, large-area electronics. It allows additive processing, thus lowering process cost. Coupled with the use of flexible substrates, printed electronics will enable a range of electronic systems, including displays, sensors and RFID tags. We review our work on the development of printed electronics. We have realised a range of printable electronic "inks", and used these to demonstrate printed active and passive components, batteries and various types of gas and biosensor. By exploiting printing to integrate these cheaply, it is likely that a range of ubiquitous electronic systems will be realised.

**Vivek Subramanian** received his MSc and PhD in electrical engineering from Stanford University, Stanford, California, in 1996 and 1998, respectively. In 1998 he co-founded Matrix Semiconductor Inc. Since 1998 he has been with the University of California, Berkeley, where he is currently an associate professor in the Department of Electrical Engineering and Computer Sciences. He has written more than 50 publications and patents. His research interests include CMOS devices and technology, and polysilicon thin-film transistor technology for displays and vertical integration applications. His current research focuses on organic electronics for display, low-cost logic and sensing applications. Subramanian has served on the technical committees for the Device Research Conference and the International Electron Device Meeting. In 2002 he was nominated to *Technology Review*'s list of top-100 young innovators and his work at Matrix Semiconductor was nominated to the *Scientific American* SA50 list for visionary technology. In 2003 he was nominated to the National Academy of Engineering's Frontiers of Engineering and was awarded an NSF Young Investigator Award.

# ESSDERC plenary talks

## Overview and Future Challenges of Floating Body Ram (FBRAM) Technology for 32 nm Technology Node and Beyond

Hamamoto, Takeshi
Toshiba Corporation

A floating body cell (FBC) is a one-transistor memory cell on an SOI substrate, which aims high density embedded memory on SOC. In order to verify this memory-cell technology, a 128 MB floating body RAM with FBC has been designed and successfully developed. The memory-cell design and the experimental results, including the single cell (one cell/bit) operation, are reviewed. Based on the experimental results, the scalability of FBC is also discussed.

**Takeshi Hamamoto** received his BSc, MSc and PhD from Waseda University, Tokyo, in 1982, 1984 and 1997, respectively. In 1984 he joined the VLSI Research Centre, Toshiba Corporation, Kawasaki, Japan, where he was engaged in research into memory-cell technologies for high-density DRAMs. From 1989 to 1992 he worked on the development of 16 Mb DRAM products, and since 1993 he has been engaged in the R&D of device and process technologies for high density/high-performance DRAMs. He has been involved in developing NAND structured DRAM cell, 6-F2 layout trench cell, embedded DRAM cell, MIM STC cell, and Fin Array FET for trench cell. At present, he is a chief specialist with the Advanced Memory Device Technology Department, Centre for Semiconductor Research and Development, and is developing the technologies for SOI and other novel memories. Dr Hamamoto is a member of the Japan Society of Applied Physics and was a subcommittee member of the Integrated Circuits and Manufacturing, International Electron Devices Meeting in 2006.

Toshiba Corporation is a high-technology, electrical engineering and electronics conglomerate based in Tokyo. It was formed in 1939 from two 19th-century telegraph and lighting companies, and it currently has 200 000 employees. It is the third largest semiconductor company in the world by sales.

## The Future of High-Performance CMOS: Trends and Requirements

Antoniadis, Dimitri
MIT

Intrinsic MOSFET time delay is examined as a function of the scaling of high-performance CMOS technology. An analytical expression is used to calculate the delay from physically meaningful transistor characteristics, which are either obtained from the literature or projected forward. The key performance parameter is the calculated virtual-source carrier velocity in the channel, which is shown to be responsible for the historical decrease in transistor delay with scaling. The forward projection of transistor delay is based on an optimistic scaling scenario with realistic assumptions about device geometry, electrostatic integrity and parasitics. It is shown that from the 32 nm CMOS generation onward the intrinsic transistor performance will not improve unless parasitic capacitances are significantly reduced. Finally, characteristics of performance scaling under localised circuit power density constraints are examined.

**Dimitri Antoniadis** received his BSc in physics from the National University of

Athens in 1970 and his PhD in electrical engineering in 1976 from Stanford University. His initial research activities were in the area of the measurement and modelling of the Earth's ionosphere and thermosphere, ranging from instrument design to computer simulation. After earning his PhD at Stanford, he led the development of the first two generations of the SUPREM process simulator, and since then his technical activity has been in the area of semiconductor devices and integrated circuit technology. He has worked on the physics of diffusion in silicon, thin-film technology and devices, and quantum-effect semiconductor devices. His current research focuses on the physics and technology of extreme-submicron Si, SOI and Si/SiGe MOSFETs. In 1978, Antoniadis joined the faculty at MIT, where he currently holds the Ray and Maria Stata chair in electrical engineering. He was co-founder and first director of the MIT Micro-systems Technology Laboratories and from 1993 to 2000 he was director of the SRC MIT Centre of Excellence for Microsystems Technology. Currently he is director of the multi-university Focus Research Centre for Materials Structures and Devices centred at MIT. He is the recipient of the Solid State Science and Technology Young Author Award of the Electrochemical Society in 1979, the Paul Rappaport Award of the IEEE in 1998 and the 2002 Andrew Grove Award of the IEEE.

## High Mobility Ge and III-V Materials and Novel Device Structures for High Performance Nanoscale MOSFETS

Saraswat, Krishna
Stanford University

In order to continue the scaling of silicon-based CMOS and maintain the historic progress in information processing and transmission, innovative device structures and new materials have to be created. A channel material with high mobility and therefore high injection velocity can increase on current and reduce delay. Currently, strained-Si is the dominant technology for high-performance MOSFETs, and increasing the strain provides a viable solution to scaling. However, looking into the future scaling of nanoscale MOSFETs, it becomes important to look at higher-mobility materials, like Ge and III-V materials, together with innovative device structures and strain, which may perform better than even very highly strained Si. For both Ge and III-V devices, problems of leakage need to be solved. Novel heterostructure quantum-well (QW) FETs will be needed to exploit the promised advantages of Ge and III-V based devices.

**Krishna Saraswat** received an MSc and a PhD in electrical engineering from Stanford University, California, in 1969 and 1974, respectively. From 1969 he was with Texas Instruments, engaged in research on microwave transistors. From 1983 he was a professor of electrical engineering at Stanford University, where he developed equipment and simulators for silicon processing. Currently he is the Rickey/Nielsen professor in the School of Engineering, professor of electrical engineering, and professor of materials science and engineering (by courtesy) at Stanford University. Since 2004 he has also been with the Birla Institute of Technology and Science as an honorary adjunct professor. He is chair of Stanford's Materials Council and on the Leadership Council of the MARCO/DARPA-funded Focus Center for Materials, Structures and Nano-Devices. Since the mid-1990s he has been engaged in research on new materials, devices, and interconnects for scaling MOS technology to sub-10 nm regime, pioneering several new concepts in 3D ICs. He has guided more than 50 doctoral students and written more than 500 technical papers. Saraswat is a recipient of the Thomas Callinan Award from the Electrochemical Society, and the 2004 IEEE Andrew Grove Award for seminal contributions to silicon process technology.

# ESSDERC tutorials

## Tutorial 1: CMOS at the Bleeding Edge

Harris Room
Organiser: Anthony O'Neill, Newcastle University, UK

This tutorial will describe state-of-the-art CMOS from both an industrial and an academic perspective. Internationally leading experts will give authoritative presentations on the current status, future directions and challenges facing advanced silicon technology. The tutorial will appeal to graduate students and young engineers who want to gain a broader perspective of the field, as well as to more experienced engineers and managers.

### Agenda

| | |
|---|---|
| 08.30 | **Introduction** A O'Neill (Newcastle University, UK) |
| 08.40 | **CMOS Scaling Into the Next Decade: An Industrial Perspective of Challenges and Opportunities** P Mahji (Intel/Sematech, USA) |
| 09.20 | **High Mobility Channel MOSFET** S Takagi (Tokyo University, Japan) |
| 10.00 | **Future Gate Stack Materials** O Engstrom (Chalmers University, Sweden) |
| 10.40 | Coffee |
| 11.00 | **Variability** A Asenov (Glasgow University) |
| 11.40 | **The SOI Mosfet: From Single Gate to Multigate** J-P Colinge (Tyndall National Institute, Ireland) |
| 12.20 | Close |

**CMOS Scaling Into the Next Decade: An Industrial Perspective of Challenges and Opportunities**
Speaker: P Mahji, Intel/Sematech

For more than three decades, CMOS scaling has provided the means to realise higher performance and lower cost/function with every technology node. This scaling, often referred to as Moore's law, has essentially allowed for a monotonic increase in density via geometric scaling while relying on conventional materials. However, as the device dimensions begin to reach the fundamental tolerance limit of conventional materials, the inevitable introduction of new materials is needed. For example, scaling below 65 nm node has seen the introduction of high-k dielectrics to curtail the increasing gate leakage. While this introduction has been characterised by Moore himself as the biggest change in transistor history in the last 40 years, it is becoming clear that many more changes involving new materials and/or architecture would be necessary to continue CMOS scaling in the future.

This work will review some of the key highlights of high-k/metal research works from various groups and provide an outlook of the primary challenges and opportunities that lie beyond advanced gate stacks, to keep up the scaling

ESSDERC TUTORIALS

roadmap beyond high-k/metal gates. More specifically, new approaches to form ultra-shallow junctions with high active dopant concentrations and low-resistance contacts with novel materials will be presented. Also, critical module level challenges for the potential replacement of Si channel with advanced high mobility channel materials (group IV and III-V) will be discussed. Generally, these high-mobility channel materials have a larger lattice constant, lower band-gap, lower thermal stability and lower dopant solubility limits. These characteristics directly challenge a) heterogeneous integration on Si platform, b) controlled short channel properties, c) formation of stable gate stacks and d) low external resistance, respectively. Trends, challenges and opportunities related to several of the aforementioned modules (gate stack, junctions, contacts, and high mobility Ge-based channels) will be briefly presented and discussed.

**High Mobility Channel MOSFET**
Speaker: Shinichi Takagi, The University of Tokyo

Channel engineering is currently recognised as mandatory for future scaled MOSFETs. Among a variety of the channel engineering, I will focus on the current drive-enhancement technologies through carrier-transport-enhanced channels using strained-Si, Ge and III-V semiconductors in this short course. I will review the basic concept of the choice of channel materials for high-performance MOSFETs, and address the critical issues for realising CMOS devices using these channel materials. I will introduce typical examples of these devices.

**Future Gate Stack Materials**
Speaker: Olof Engstrom, Chalmers University, Sweden

The dielectric material of MOSFET gate stacks has two main purposes: (1) to keep the electric vector field in the transistor channel under control and (2) to limit the gate leakage current. The former requirement means that the capacitive coupling between the gate metal and the channel must be high, which in turn involves the need for a thin dielectric layer. For an ideally amorphous or monocrystalline dielectric, the leakage is determined by tunnelling. This, however, requires a thick dielectric or a high value of the “equivalent oxide thickness” (EOT), which can be achieved by a high dielectric constant, k. Also, a high energy offset valuẹ,✣E, between the energy bands of the semiconductor and the dielectric limits leakage by tunneling. As a rule of thumb, in order to fulfil a given field versus leakage requirement, k and ✣E approximately need to combine to a minimum product k x ✣⁜✝CE. For the 22 nm LSTP bulk node and beyond, it is estimated that CE should be about 70 eV and above, while for SOI technology this value may be lower. In a CMOS process, there are a number of obstacles to achieve materials with the ideal properties mentioned above, including chemical stability, interface properties and charge carrier traps. Moreover, being influenced also by the properties of the gate metal, the dielectric cannot be treated separately. The whole gate stack, therefore, must be considered with a holistic approach. In present gate stack development the bearing is set on rare-earth metal oxides and on ternary compounds based on rare-earth elements. Describing these problems as a background, the talk will discuss the prospects of finding gate stack combinations to fulfil the requirements of future CMOS technology.

**Variability**
Speaker: Asen Asenov, University of Glasgow

The variability of the transistor characteristics has become a major concern associated with CMOS transistors scaling and integration. It already critically

affects SRAM scaling, and introduces leakage and timing issues in digital logic circuits. The variability is the main factor restricting the scaling of the supply voltage, which for the last three technology generations has remained constant, adding to the looming power crisis.

The tutorial will introduce the different sources of variability on CMOS including process control and uniformity related variability, systematic (deterministic) lithography and stress related variability and statistical variability associated with the discreteness of charge and granularity of matter. The main focus of the tutorial will be on the statistical variability, which has become a dominant source of variability at the 45 nm technology generation and which cannot be reduces by tightening the process control. While in the case of systematic variability the impact of lithography and stress on the characteristics of an individual transistor can be modelled or characterised and therefore factored in the design process, in the case of statistical variability only the statistical behaviour of the transistors can be simulated or characterised. Two macroscopically identical transistors next to each other can have characteristics from the two distant ends of the statistical distribution.

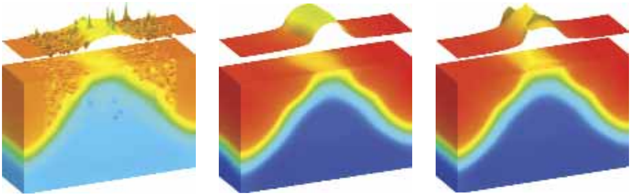


*Fig. 1: Random discrete dopants in a 35 nm MOSFET. Fig. 2: Line edge roughness in a 35 nm MOSFET. Fig. 3 Poly Si granularity in a 35 nm MOSFET.*

In the tutorial we will review the major sources of statistical variability in nano CMOS transistors focusing at the 45 nm technology generation and beyond. The dominant sources of statistical variability including random discrete dopants (Fig.1), like edge roughness (Fig. 2) and poly silicon granularity (Fig. 3) will be discussed in details.

**The SOI MOSFET: From Single Gate to Multigate**
Speaker: Jean-Pierre Colinge
Tyndall National Institute, Cork, Ireland

The classical MOSFET is reaching its scaling limits and "end-of-roadmap" alternative devices are being investigated. In a continuous effort to increase current drive and better control short-channel effects, silicon-on-insulator MOS transistors have evolved from classical, planar, single-gate devices into three-dimensional devices with a multi-gate structure (double-, triple- or quadruple-gate devices). It is worth noting that, in most cases, the term "double gate" refers to a single gate electrode that is present on two opposite sides of the device. Similarly, the term "triple gate" is used for a single gate electrode that is folded over three sides of the transistor. This lecture describes the evolution of MOS transistors from single-gate to multiple-gate structures, the associated benefits and potential problems of this technology migration, as well as the emergence of novel quantum effects in small multigate devices.

### Biographies

**Anthony O'Neill** was born in Leicester, England in 1959. He received the BSc degree from the University of Nottingham in 1980 and the PhD degree from the University of St Andrews three years later. Between 1983 and 1986 he worked for Plessey Research (Caswell) Ltd before taking up his post at the University of

Newcastle upon Tyne. He has worked on a wide range of topics in the field of semiconductor device and process technology and published many papers. In 1994 he was Visiting Scientist at MIT (Microsystems Technology Laboratories) and in 2002 he became a Royal Society Industry Fellow with Amtel. He was appointed to a personal chair in physical electronics and since 1996 has been Siemans Professor of Microelectronics. He is an IEEE Distinguished Lecturer, a Fellow of the IET and a director of the National Microelectronics Institute, UK. Current research interests include Si, strained Si/SiGe and SiC device and process technologies and interconnect reliability. He is the chair for tutorials and workshops at ESSDERC 2008.

**Prashant Majhi** received his Bachelors of Technology degree from the Indian Institute of Technology, Madras (1996), and his PhD in science and engineering of materials program from Arizona State University, Tempe, AZ (2000). He joined Phillips Semiconductor in the Netherlands and worked on several CMOS and mixed-signal process technologies. In 2004, he joined Intel Corp., and is currently at SEMATECH as an Intel Assignee managing the CMOS scaling group.

**Shin-ichi Takagi** was born in Tokyo, Japan, on 25 August 1959. He received a BSc, an MSc and a PhD in electronic engineering from the University of Tokyo, Tokyo, Japan, in 1982, 1984 and 1987, respectively. His PhD thesis involved the study on the surface carrier transport in MISFETs based on III-V semiconductors. He joined the Toshiba Research and Development Center, Kawasaki, Japan, in 1987, where he has been engaged in the research on the device physics of Si MOSFETs, including the carrier transport in the inversion layer, the impact ionisation phenomena, the hot carrier degradation and the electric properties of $Si/SiO_2$ interface. From 1993 to 1995, he was a Visiting Scholar at Stanford University, Stanford, California, where he studied the Si/SiGe hetero-structure devices. Since returning to the ULSI Research Laboratories, he was also engaged in the physics and technology of the reliability of $SiO_2$, ferroelectric devices and strained- Si MOS devices. From 2001 to 2008, he worked for the MIRAI Project, as the leader of Ultra-High Performance New Transistor Structures Theme. In October 2003, he moved to the University of Tokyo, where he is currently working as a professor in the department of Electronic Engineering, School of Engineering. His recent interests include the science and the technologies of advanced Si CMOS and high performance CMOS devices using new channel materials, such as strained-Si, Ge and III-Vs. Dr Takagi served on the technical programme committee on several international conferences, including the International Electron Device Meeting, the International Reliability Physics Symposium, the International Conference on Solid State Device and Materials, and the International Solid State Circuits Conference. He is a member of the IEEE Electron Device Society and the Japan Society of Applied Physics.

**Olof Engström** received a PhD in solid-state physics from the University of Lund in 1975 and was later employed by ASEA AB for research on high-power thyristors, by AB Rifa for development of MOS technology and by the Swedish Defence Research Institute for sensor research. In 1984 he came to Chalmers University of Technology as a professor in solid-state electronics. Between 1996 and 1999 he served as dean of Chalmers School of Electrical and Computer Engineering, and from 1999 to 2002 he was director of the Microtechnology Center at Chalmers (MC2). Since 2003 he has been back in research as a professor at the Department of Microtechnology and Nanoscience of MC2. His present research interest is in high-k-materials and semiconductor quantum structures. In 1991 he founded Samba Sensors AB, a company for the production of fibre-optical pressure sensors. He is a member of the Royal Swedish Academy of Engineering Science, the Finnish Society of Science and

the High-k-Gang (**www.high-k-gang.eu**).

**Asen Asenov** received his MSc in solid-state physics from Sofia University, Bulgaria, in 1979 and a PhD in physics from The Bulgarian Academy of Science in 1989. He is a professor of Device Modelling, leader of the Glasgow Device Modelling Group and academic director of the Glasgow Process and Device Simulation Centre. He coordinates the development of 2D and 3D quantum mechanical, Monte Carlo and classical device simulators and their application in the design of advanced and novel CMOS devices. He has pioneered the simulations of statistical variability in nano-CMOS devices, interface roughness and line-edge roughness. He has more than 450 publications in the above areas.

**Jean-Pierre Colinge** received a BSc in philosophy, an electrical engineering degree and a PhD in applied sciences from the Université Catholique de Louvain, Louvain-la-Neuve, Belgium, in 1980, 1980 and 1984, respectively. He has worked at the Centre National d'Etudes des Télécommunications (CNET), Meylan, France, at the Hewlett-Packard Laboratories, Palo Alto, USA, and at IMEC, Leuven, Belgium, where he was involved in SOI technology for VLSI and special device applications. From 1991 to 1997, Colinge was professor at the Université catholique de Louvain, leading a research team in the field of SOI technology for low-power, radiation-hard, high-temperature and RF applications as well as reduced-dimension devices (thin double-gate and quantum-wire MOSFETs). From 1997 to 2006 he was professor at the University of California at Davis, carrying on research on advanced multigate SOI MOS devices. He has been on the committee of several conferences, including IEDM and SSDM, has been general chairman of the IEEE SOS/SOI Technology Conference in 1988, and is a fellow of IEEE. He has published more than 300 scientific papers and four books on the field of SOI, as well as two books on semiconductor device physics. Colinge is currently professor at the Tyndall National Institute, Ireland, where he is working on the modelling, fabrication and characterisation of advanced SOI MOS devices.

## Tutorial 2: Characterisation for the Nanoelectronics Era

Ochill Room
Organiser: Herman Maes

One of the objectives of the PULLNANO IP-project is to organise training sessions and courses for researchers and engineers in Europe, based on the know-how built up within this project.

The ESSDERC/ESSCIRC 2008 conference has been considered to be a very suited forum for such a contribution from PULLNANO and more in particular in the area of characterisation of nanometer technologies and devices on which significant achievements were realised in the course of this project. The topics that were selected are related to very challenging issues in the development of nanometer technologies and devices. These include the characterisation of high-k materials, the characterisation of shallow junctions and the modelling and characterisation of stress and strain. We are pleased to offer a very exciting Tutorial program involving an elite group of lecturers who are experts in their field and also excellent teachers and who will give a general introduction in their area of competence complemented with results from the related research activities within PULLNANO.

This tutorial session offers an excellent introduction to the relevant issues and is therefore strongly recommended and is in fact a "must" not only for those who are starting in this field but also for all physicists and engineers who want to get

familiar with the characterisation issues in these nanometre devices.

We look forward to welcoming you in the Tutorial session in Edinburgh.

**Agenda**

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|---|---|
| 13.45–14.00 | **Welcome and introduction to the tutorial session** Anthony O'Neil, Newcastle University, UK & Herman E. Maes, IMEC, Leuven, Belgium |
| 14.00–14.45 | **Introducing Characterisation and Metrology** Tom Stevenson, University of Edinburgh, UK |
| 14.45–15.30 | **Physical Characterisation of High-K Materials** Christophe Wyon, STMicroelectronics, France |
| 15.30–16.00 | Coffee break |
| 16.00–16.30 | **Two-dimensional Carrier Profile Characterisation for Junction Engineering in Advanced Devices** Pierre Eyben and Wilfried Vandervorst, IMEC, Belgium |
| 16.30–17.15 | **Strain Measurements in Layers and Devices** Alain Claverie, CEMES, France |
| 17.15–18.00 | **Process Simulation for Advanced Stress and Junction Engineering** Christophe Krzeminski and Evelyne Lampin, IEMN, France |
| 18.00 | End of session |

**Introducing Characterisation and Metrology**
Speaker: Tom Stevenson, University of Edinburgh, UK

The tutorial will provide an introductory review of the major metrology techniques which are used in the microfabrication of devices on silicon, for both conventional circuits and MEMS devices. When a layer of material is grown or deposited, process engineers need to monitor and control layer thickness, composition, stress, surface finish, and optical properties. The subsequent photolithography process has its own set of measurements including resist thickness, critical dimensions (CD) and layer to layer registration (overlay). The etch process will again require CD measurement as well as layer thickness or etch depth. As dimensions have shrunk on conventional devices, metrology techniques have had to change in order to resolve and measure the smaller features (CD) and thinner layers. On MEMS devices, the critical dimensions may still be relatively large and amenable to optical imaging but this approach may be difficult when layers are tens or hundreds of microns thick. The tutorial will conclude by highlighting some of the major metrology challenges which are predicted by the roadmap.

**Physical Characterisation of High-K Materials**
Speaker: Christophe Wyon, STMicroelectronics, France

In the frame of the European PullNano project, several techniques for the chemical and morphological characterisation of advanced gate stacks, and in particular the high κ dielectric, have been investigated. Several practical aspects of scanning transmission electron microscopy-electron energy loss

spectroscopy (STEM-EELS) and other TEM methods in the application to gate stacks were addressed. High κ/metal gate process was accurately characterised using synchrotron radiation-X-ray photoelectron spectroscopy (SR-XPS). SR-XPS enables the characterisation of buried thin films like interfacial layers, which usually occur in the high κ process. The on-line monitoring of high κ related processes was successfully achieved using X-Ray Reflectivity (XRR) technique.

**Two-dimensional Carrier Profile Characterisation for Junction Engineering in Advanced Devices**
Speaker: Pierre Eyben, IMEC, Leuven, Belgium

Junction engineering in advanced devices is a complex task as it requires a complete understanding of all possible 1D and 2D interactions and the interplay between preamorphisation steps, halo-implants and LDD/HDD profiles but equally the impact of (outdiffusion into) liners, details of the gate profile and implant tilt, pile-up during silicidation, stress effects on diffusion and activation etc. Due to this complexity simple 1D-experiments are no longer adequate and only true 2D-carrier (and dopant) profiles will provide the required fundamental understanding. The requirements on the characterisation techniques for 2D-profiling are very stringent as one needs to combine sub-nm spatial resolution, with a high sensitivity (covering the entire concentration range of interest), and accurate quantification. Within the PULLNANO project Scanning Spreading Resistance Microscopy (SSRM) has emerged as the sole method able to fulfil all these requirements with a resolution as small as 0.5 nm. In this presentation we will discuss the basic aspects of SSRM, demonstrate its compliance with all (ITRS)-requirements and demonstrate its application for process development and TCAD calibration on planar and FINFET devices.

**Strain Measurements in Layers and Devices**
Speaker: Alain Claverie, CEMES, France

While stress in chips has been for long an undesirable effect resulting from processing and/or packaging, strained silicon is now an integral feature of the latest generation of transistors and electronic devices because of the associated enhancement in carrier mobility. Different strategies have been used to engineer strain in devices, leading to complex strain distributions in two and three dimensions. Developing methods of strain measurement at the nanoscale has therefore been an important objective in recent years but has proved elusive in practice: none of the existing techniques combines the necessary spatial resolution, precision and field of view. For example, Raman spectroscopy or X-ray diffraction techniques can map strain at the micrometer scale, whereas transmission electron microscopy allows strain measurement at the nanometer scale but only over small sample areas. Along this tutorial, we will review and discuss the applicability of these different techniques through technologically relevant examples and present a recently invented technique capable of bridging this gap and measuring strain to high precision, with nanometre spatial resolution and for micrometer fields of view.

**Process Simulation for Advanced Stress and Junction Engineering**
Speaker: Christophe Krzeminski and Evelyne Lampin, IEMN, France

For CMOS devices downscaling, sharp requirements have been defined by the International Technology Roadmap for Semiconductors (ITRS) in terms of drive and off state current and power density, making the geometric scaling a challenging task. The new vector largely adopted to extend Moore’s law is the mobility enhancement through the introduction of stress by several techniques

(Stress Liner, eSiGe embedded stressor, stress memorisation). On the other side, a challenging experimental trade-off is being made on jonction processing to meet the sharp requirements in terms of resistance, abruptness and depth. Standard techniques (implantation and rapid thermal annealing) are being pushed to their limits whereas alternative techniques such as preamorphisation, solid phase epitaxy (SPE), laser annealing and plasma doping are being optimised. As will be shown in this session of PULLNANO tutorials, many challenges are being faced by characterisation methods and metrology to support all of this intense research competition. TCAD more generally, and process simulation in particular, have a complementary role to play to identify trade-off and evaluate the scalability. The progresses recently made by standard finite element based simulators for the modelling of implantation, diffusion and stress engineering will be reviewed and illustrated by examples from different european projects and from the literature. Furthermore, as the complexity increases with device downscaling, atomistic simulations are of interest to provide more understanding and to perform computer experiments in cases where the time or atomic scale are very challenging for characterisation. Several examples from our recent research work with molecular dynamics in PULLNANO will be presented.

### Biographies

**Tom Stevenson** is operations director of the Scottish Microelectronics Centre, University of Edinburgh, responsible for all aspects of cleanroom operations. He is also active, in a technical capacity, in a number of research areas, ranging from novel device structures to CMP for MEMS devices. His interest in metrology dates back to 1969, when he studied instrument design at the University of Aberdeen (MSc) and thereafter spent five years at Ferranti Ltd, Dalkeith, as a development engineer on moire fringe measuring systems for machine tools and co-ordinate-measuring machines. At the University of Edinburgh his main research interests have been in optical lithography and metrology associated with microfabrication of both microelectronic and MEMS devices.

**Christophe Wyon** has been manager of the ST Crolles Physical Characterisation department since 2002. After receiving a PhD in surface physics and chemistry from the National Polytechnique Institute of Grenoble, he joined CEA-LETI for working on crystal growth of dielectric materials. In 1990 he managed the crystal growth laboratory before taking the head of Thermal processes and wet chemistry in the Microelectronics Department in 1997. In 1999 Christophe Wyon was in charge of the Physical and Chemical Characterisation laboratory at CEA-LETI. Christophe Wyon led several European projects devoted to the physical and chemical characterisation and metrology of advanced CMOS processes. He is author and co-author of more than 55 international papers.

**Pierre Eyben** was born in 1975, obtained his MSC in engineering in 1998 (Université Liege) and in 2004 his PhD at the K U Leuven with a thesis entitled "Scanning spreading resistance micrsocopy: high-resolution two-dimensional carrier profiling of semiconductor structures". From 2004 to 2006 he worked as a postdoctoral fellow from the IWT (Flemish Institute for Science and Technology) at IMEC on the further implementation of SSRM and joined Imec in 2006, where he is now responsible for the SSRM research and service activities.

**Wilfried Vandervorst** was born in 1954, obtained his MSc in engineering in 1977 and a PhD in 1984 (K U Leuven). He joined IMEC in 1985, where he is currently heading the Materials and Components Analysis Group. In 1990 he also became a professor at the K U Leuven and was nominated as Imec fellow in 2001. His prime research is currently focused on the development of metrology concepts for the characterisation of advanced devices with a special

emphasis on approaches with high 2D/3D resolution.

**Alain Claverie** obtained a Dipl Ing in solid-state physics in 1981 from the National Institute for Applied Science (INSA) of Toulouse, then a PhD in 1984 from the University Paul Sabatier of Toulouse. From 1985 he was staff scientist (permanent position) in the semiconductor group at CEMES, an autonomous laboratory of the National Center for Scientific Research, where he performed experimental work on the TEM characterisation of ion implanted materials. From 1988 to 1993 he was visiting or staff scientist in national laboratories abroad, notably in India (Chandigarh) and California (Berkeley). Claverie's interests range from the nucleation and growth of extended defects and nanoprecipitates, diffusion anomalies in semiconductors and very low energy ion implantation. He is the author or co-author of more than 150 publications in international journals and serves as a regular reviewer for *APL*, *JAP*, *PRL*, *PR* and *Nature Materials*. He has been the organiser of several international conferences (MRS (3), E-MRS (3), IEEE, GADEST) and is a member of the scientific/technical boards of several others. Recently he was the coordinator of the EC-supported NEON (nanoparticles for electronics) a GROWTH Project aimed at engineering nanocrystals for memory applications. Appointed as directeur de recherches in 2002, he is now in the charge of nanoMaterials Group he created at CEMES, where about 30 permanent scientists and about the same number of postgraduates and postdocs work on the synthesis, physics, characterisation and integration of nanocrystals and ultrathin films in systems for applications in electronics, magnetism and optics. E-mail him at claverie@cemes.fr.

**Christophe Krzeminski** was born in 1975. He received an engineering degree from the Institut Supérieur d'Electronique et du Numérique in 1998 and a PhD in electronics from the University of Lille in 2001. From 1998 to 2001 he was involved in the modelling of electronic transport in molecular nanometric electronics devices. In 2001 he joined the institute d'Electronique, de Microelectronique et de Nanotechnologie (IEMN) as an assistant professeur in the Silicon Microelectronics Department. His research was first focused on the development of a new approach to silicon oxidation and oxynitridation modelling. In 2003 he joined the Centre de la Recherche Scientifique (CNRS) as a research scientist. His current interests concern the simulation and optimisation of nanodevices, and the development of continuous and atomistic models for silicon process simulation.

**Evelyne Lampin** (née Martin) is in charge of research at the french National Center of Scientific Research (CNRS). She is working at the Institute of Electronic, Microelectronic and Nanotechnology (IEMN) close to Lille. She received an engineering degree from ISEN in 1994 and a PhD in material science from the University of Lille in 1997. Her dissertation dealt with the calculation of the electronic states and of the dynamic of carriers in silicon nanostructures. She joined the Silicon Microelectronic Group of the IEMN in 1997, where she is studying the physics of advanced silicon technology. Her particular interest is the modelling of dopant diffusion and activation. After developing continuous models of the extended defects formed by ion implantation, she is now using atomistic methods to study the recrystallisation of silicon after amorphising implants.

## Tutorial 3: Integrating CMOS with other Technologies

PM Moorfoot Room
Organiser: Jon Terry

The evolution of silicon microelectronics has seen a recent diversification into new device types and associated novel application areas. Examples of this

diversification include smart power, RF systems, microsystems, microdisplays, bioelectronics and silicon photonics. These technologies have in common the use of silicon as a platform for system integration with the added value being the innovation associated with post-processing of, in many cases, standard foundry technology. These so-called Silicon+ technologies will most likely become the mainstream silicon research direction when scaling has run its course and hits a combination of technological and economic barriers.

In this tutorial, experts in academia, start-up technology companies and international semiconductor manufacturers will examine the challenges involved in this exciting field. Existing and potential solutions will be presented and future difficulties discussed. A number of case-studies from industry at the forefront of this stimulating area will provide invaluable first-hand experience. The tutorial will appeal to graduate students and young engineers, as well as to more experienced engineers and managers who are looking for an informal and informative introduction to this important field.

### Agenda

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|---|---|
| 13.30–14.10 | **Introduction to Integrating CMOS with other Technologies** Anthony Walton, University of Edinburgh, UK |
| 14.10–14.50 | **Design for Manufacture Challenges in MEMS enabled Micro & Nano Systems** Andrew Richardson, Lancaster University, UK |
| 14.50–15.30 | **Post-Processing Microdisplays on CMOS** Ian Underwood, Microemissive Displays, UK |
| 15.30–15.50 | Coffee break |
| 15.50–16.30 | **Post-processing Image Sensors on CMOS** Lindsay Grant, ST Microelectronics, UK |
| 16.30–17.10 | **CMOS Integration with Biotechnology** Roland Thewes, Qimonda, Germany |
| 17.10–17.50 | **Gas Multiplication Grid Integrated on CMOS** Jurriaan Schmitz, University of Twente, Netherlands |
| 17:50 | Close |

**Introduction to Integrating CMOS with other Technologies**
Speaker: Anthony Walton, University of Edinburgh, UK

The mainstream IC industry, manufacturing devices such as memories and microprocessors, follows the ITRS roadmap towards smaller and smaller devices. However, in parallel, there is increasing activity involving the integration of silicon with other technologies and new materials, and it is clear that MEMS will form an important component of this Silicon+ activity. This tutorial provides an introduction and identifies the options available for integrating MEMS with IC technology with examples being used to identify some of the issues associated with their implementation.

**Design for Manufacture Challenges in MEMS enabled Micro & Nano Systems**
Speaker: Andrew Richardson, Lancaster University

Design for Manufacture technology has been prioritised, developed and used within the microelectronics community to optimise yield, customise designs to specific processes and optimise both testability and reliability. MEMS integration through wafer level packaging and system-in-package technology opens new challenges within these fields. This presentation will discuss the design challenges that relate to manufacturability that need to be addressed before routine integration of MEMS into electronic systems can be achieved. Emerging Design-for-X methods including "DfTestability", "DfReliability" and "DfYield" will be covered with examples of how these techniques can be applied within a systems engineering environment.



**Post-processing Microdisplays on CMOS**
Speaker: Ian Underwood, Microemissive Displays, UK

This tutorial will broadly review the integration of arrays of light controlling elements on CMOS substrates. It will cover the applications, capabilities and process requirements of a number of distinct technologies each of which either emits or modulates light. The particular application of microdisplays will be a theme of the tutorial.

**Post-processing Image Sensors on CMOS**
Speaker: Lindsay Grant, ST Microelectronics, UK

This tutorial will broadly review the integration of arrays of light sensing elements on CMOS substrates. It will cover the technology behind a range of light sensing technologies and the processing involved in their integration with other technologies. A specific theme of the presentation will be the development and fabrication of CMOS light sensors used in camera chips.

**CMOS Integration with Biotechnology**
Speaker: Roland Thewes, Qimonda, Germany

There has been significant interest recently with the fabrication of electronic systems for biotechnology research; terms such as lab-on-a-chip (LOC) have found their way into everyday use. This tutorial will examine the various technologies involved in the fields of bio molecule detection and nerve cell/neural tissue interaction and discuss related advantages and challenges in accuracy, sensitivity and time-to-result, which have been achieved by the integration of CMOS control and sensing circuitry with the wet world of biotechnology

**Gas multiplication grid integrated on CMOS**
Speaker: Jurriaan Schmitz, University of Twente, Netherlands

This final tutorial will take the form of a case-study examining the technology which has been developed to allow a CMOS (pixel) readout chip to be integrated with a gas multiplication grid. The resulting system forms an integrated device that can be applied as a readout device applicable to the increasingly important field of gaseous detectors.

## Biographies

**Anthony Walton** is professor of microelectronic manufacturing in the School of Engineering and Electronics at the University of Edinburgh. He leads the technology research activities in the Institute for Integrated Micro and Nano Systems (IMNS) and was instrumental in setting up the Scottish Microelectronics Centre (SMC). This is a purpose-built facility for R&D and company incubation consisting of approximately 350 $m^2$ of class-10

cleanrooms. His research interests include the design and fabrication of microsystem technology and its integration with CMOS, which has been a feature of many of the companies that have been spun out of the IMNS. He has published more than 200 papers, he is an associate editor of the IEEE's *Transactions on Semiconductor Manufacturing* and a member of the IEEE.

**Andrew Richardson** currently holds a personal chair in microsystems engineering in the Department of Engineering at Lancaster University. He is director of the Centre for Microsystems Engineering and scientific director of Dolphin Integration, Grenoble. He has published 140 journal, conference and workshop papers, together with two books that cover work in the fields of mixed signal and analogue design-for-test, defect, fault and degradation modelling, MEMS modelling, and test and design for micro and nanomanufacture. More recently he has been carrying out work on system-in-package technology, multisensor microsystems for health monitoring applications, and both bio-MEMS and microfluidics. Richardson has contributed to funded projects in all European IST programmes since 1994. This includes the coordination of the FP6 PATENT-DfMM Network of Excellence that involves 24 partners and more than 140 researchers across 10 European countries. He is also a partner in the QinetiQ-led integrated project Integrated MNT Platforms & Services (INTEGRAMplus) and is a co-investigator and member of the management team for the EPSRC Innovative Electronics Manufacturing Centre. Richardson is also a steering committee member for the NEXUS Association that represents European universities and industry working in the field of integrated MEMS.

**Ian Underwood** is a co-founder of MED and co-inventor of its P-OLED microdisplay technology. Prior to 1999 he was at the University of Edinburgh, where he carried out pioneering research and development R&D in the field of liquid-crystal microdisplays between 1983 and 1999. He is a Fulbright fellow (1991), Photonics Spectra Circle of Excellence designer (1994), British Telecom fellow (1997), Ben Sturgeon Award winner (1999), Ernst & Young Entrepreneur of the Year (2003), fellow of the Royal Society of Edinburgh (2004), Gannochy Medal winner (2004), fellow of the Royal Academy of Engineering (2008) and fellow of the Institute of Physics (2008). As chief scientific advisor he is responsible for putting in place projects and programmes to ensure that MED's future products will continue to meet the challenge of fast-moving markets and innovative customers. He is recognised worldwide as an authority on microdisplay technology, systems and applications. In 2005, Underwood was made professor of electronic displays at the University of Edinburgh. In addition to his full-time post at MED, he sits on the Council of the Scottish Optoelectronics Association and the Steering Committee of ADRIA (Europe's Network in Advanced Displays). He is co-author of a recently released book entitled *Introduction to Microdisplays*.

**Lindsay Grant** was born in Glasgow, Scotland, in 1961. He received a BSc in physics from St Andrews University in 1984 and embarked on a career in the semiconductor industry. He has more than 20 years' experience in semiconductor device physics and process development. Initially he worked near Bristol, UK, for equipment manufacturer Electrotech on plasma etch processing. Then, having moved to Harlow, UK, he spent three years in device engineering with STC working on BiCMOS process development. Returning to Scotland in 1988 he spent 11 years with Seagate Microelectronics, Livingston. There he worked on bipolar, CMOS, DMOS and BiCMOS technologies and he held positions in product, device and process engineering. In 1999 he joined ST Microelectronics, Edinburgh. ST acquired VLSI Vision in 1999 and, since then, Grant has played a key role in the development and introduction of CMOS Image Sensor process technology inside ST. He has worked on the development

of seven generations of pixel technology with ST progressing from 5.6 μm pitch in 1999 to 1.4 μm in 2008. He currently holds the position of imaging process development manager in the Imaging Division. He has written several papers on imaging technology and been an invited speaker at imaging conferences.

**Roland Thewes** was born in Marl, Germany, in 1962. He received his PhD in electrical engineering from the University of Dortmund, Germany, in 1995. In 1994 he joined the research laboratories of Siemens AG, where he was active in the field of reliability and yield of analogue CMOS circuits, and in the design of non-volatile memories. From 1997 to 1999 he managed projects in the areas of design for manufacturability, reliability, analogue device performance and analogue CMOS circuit design. From 2000 to 2005 he was responsible for the Lab on Mixed-Signal Circuits of Corporate Research of Infineon Technologies, focusing on CMOS-based biosensors, analogue CMOS circuit design and device-circuit interaction. Since 2006 he has been responsible for DRAM core circuitry development at Qimonda. Moreover, he serves as a consultant of the Max-Planck Society in the area of CMOS-based neural tissue imaging. He has written or co-written some 130 technical publications and a similar number of granted patents and patent applications. He has served as a member of the technical programme committees of various conferences. Currently he is a member of the technical program committees of ISSCC and ESSDERC, of the executive committee of IEDM, and of the joint steering committee of ESSDERC/ESSCIRC.

**Jurriaan Schmitz** (1967) obtained his MSc (1990) and PhD (1994) at the University of Amsterdam in the field of experimental high-energy physics carried out at NIKHEF. His PhD thesis, supervised by Prof. Jos Engelen, dealt with the R&D of the microstrip gas counter, with the intent to apply it in the ATLAS inner detector. After his PhD he joined Philips Research (in Eindhoven, Netherlands) to work on CMOS transistor downscaling, and the characterisation and reliability of MOS devices. Since 2002 he has been a full professor at the University of Twente. At present he heads a group of 25 people devoted mainly to scientific research on the components inside integrated circuits. His current research programme focuses on CMOS post-processing techniques, details of which can be found at http://sc.el.utwente.nl/research. He holds 14 US patents and has written or co-written more than 80 scientific papers. He is a member of the IEEE and the Dutch and European Physical Societies.

# ESSDERC programme

## Tuesday September 16

| | |
|---|---|
| 08.50 | **Introduction to ESSDERC and ESSCIRC 2008** |
| **A1L-A**<br>Pentland<br>Chair(s): | **Joint plenary** R. Chau<br><br>Anthony Walton, University of Edinburgh<br>Stephen Hall, University of Liverpool |
| **A1L-A1**<br>09.00 | **Emerging Device Nanotechnology for Future High-Speed and Energy-Efficient VLSI: Challenges and Opportunities**<br>Robert Chau, Intel Corporation, USA |
| **A2L-A**<br>Pentland<br>Chair(s): | **Process Variablilty and Yield** Joint session<br><br>Asen Asenov, University of Glasgow |
| **A2L-A1**<br>09.50<br>Author(s): | **Experimental Assessment of Logic Circuit Performance Variability with Regular Fabrics at 90 nm Technology Node**<br>Sungdae Choi, University of Tokyo; Katsuyuki Ikeuchi, University of Tokyo; Hyunkyung Kim, University of Tokyo; Kenichi Inagaki, University of Tokyo; Masami Murakata, Semiconductor Technology Academic Research Center; Nobuyuki Nishiguchi, Semiconductor Technology Academic Research Center; Makoto Takamiya, University of Tokyo; Takayasu Sakurai, University of Tokyo |
| **A2L-A2**<br>10.10<br>Author(s): | **Area/Yield Trade-Offs in Scaled CMOS SRAM Cell**<br><br>Vasudha Gupta, Mohab Anis, University of Waterloo |
| **A2L-A3**<br>10.30<br>Author(s): | **Evaluation of Intrinsic Parameter Fluctuations on 45, 32 and 22nm Technology Node LP N-MOSFETs**<br>Binjie Cheng, Scott Roy, Andrew Brown, Campbell Millar, Asen Asenov, University of Glasgow |
| **A2L-B**<br>Fintry<br>Chair(s): | **Reliability**<br><br>Dimitris Tsoukalas, National Technical University of Athens<br>Reinout Woltjer, NXP |
| **A2L-B1**<br>09.50<br>Author(s): | **A 65 nm Test Structure for the Analysis of NBTI Induced Statistical Variation in SRAM Transistors**<br>Thomas Fischer, Technische Universität München; Ettore Amirante, Karl Hofmann, Martin Ostermayr, Peter Huber, Infineon Technologies AG; Doris Schmitt-Landsiedel, Technische Universität München |
| **A2L-B2**<br>10.10<br>Author(s): | **An Equivalent Circuit Model for the Recovery Component of BTI**<br>Javier Martin-Martinez, Rosana Rodriguez, Montse Nafria, Xavier Aymerich, Universitat Autònoma de Barcelona; Ben Kaczer, Guido |

Groeseneken, IMEC

**A2L-B3** — **New Floating-Body Effect in Partially Depleted SOI pMOSFET Due to Direct-Tunneling Current in the Partial N+ Poly Gate**
10.30
Author(s): Georges Guegan, Romain Gwoziecki, Patricia Touret, Christine Raynaud, Simon Deleonibus, CEA LETI – MINATEC; Jeremy Pretet, Olivier Gonnard, Gilles Gouget, STMicroelectronics

**A2L-C** — **High Voltage Devices**
Sidlaw
Chair(s): Mikael Ostling, KTH
Giles Dambrine, IEMN

**A2L-C1** — **High-Voltage Trenched Rectifiers for Smart Power Technology**
09.50
Author(s): Jaume Roig, Bart Desoete, Peter Moens, Filip Bauwens, On Semiconductor

**A2L-C2** — **DC-Arc Behavior of a Novel Active Fuse**
10.10
Author(s): Joachim Vom Dorp, Friedrich-Alexander University Erlangen-Nuremberg; Sven Berberich, Anton Bauer, Fraunhofer Institute of Integrated Systems and Device Technology; Heiner Ryssel, Friedrich-Alexander University Erlangen-Nuremberg

**A2L-C3** — **Design of Rugged High Voltage High Power P-Channel Silicon MOSFET for Plasma Applications**
10.30
Author(s) Jinshu Zhang, Dumitru Sdrulla, Dahwen Tsang, Dick Frey, George Krausse, Microsemi Corporation

10.50 Coffee break

**A3L-B** — **Channel Engineered Devices**
Fintry
Chair(s): Thomas Ernst, CEA LETI
Kristin De Meyer, IMEC

**A3L-B1** — **High Performance 70 nm Gate Length Germanium-On-Insulator pMOSFET With High-/Metal Gate**
11.20
Author(s): Krunoslav Romanjek, CEA LETI – MINATEC; Louis Hutin, CEA LETI; Cyrille Le Royer, CEA LETI – MINATEC; Arnaud Pouydebasque, Marie-Anne Jaud, CEA LETI; Claude Tabone, CEA LETI – MINATEC; Emmanuel Augendre, Loic Sanchez, Jean-Michel Hartmann, CEA LETI; Helen Grampeix, CEA LETI – MINATEC; Vincent Mazzochi, Sébastien Soliveres, Roland Truche, Laurent Clavelier, Pascal Scheiblin, CEA LETI

A3L-B2 — **Ge p-channel MOSFETS with $La_2O_3$ and $Al_2O_3$ Gate Dielectrics**
11.40
Author(s): Christophe Rossel, IBM Research GmbH, Zurich Research Laboratory; Athanasis Dimoulas, NCSR DEMOKRITOS; Axelle Tapponnier, Daniele Caimi, David Webb, Caroline Andersson, Marilyne Sousa, Chiara Marchiori, Heinz Siegwart, Jean Fompeyrine, Roland Germann, IBM Research GmbH, Zurich Research Laboratory

**A3L-B3** 12.00
**Atomically Flat Gate Insualtor/Silicon (100) Interface Formation Introducing High Mobility, Ultra-low Noise, and Small Characteristics Variation CMOSF**
Author(s): Rihito Kuroda, Akinobu Teramoto, Tomoyuki Suwa, Rui Hasebe, Xiang Li, Masahiro Konda, Shigetoshi Sugawa, Tadahiro Ohmi, Tohoku University

**A3L-B4**
**Poly-Si Stripe TFTs by Grain-Boundary Controlled Crystallization 12.20 of Amorphous-Si**
Author(s): Ihor Brunets, Jisk Holleman, Alexey Kovalgin, Jurriaan Schmitz, MESA Institute for Nanotechnology, University of Twente

**A3L-C** Sidlaw
**Advanced Analogue and RF Devices**
Chair(s): Peter Ashburn, University of Southampton
Stefaan Decoutere, IMEC

**A3L-C1** 11.20
**Monolithic Integration of CMOS VLSI and CNT for Hybrid Nanotechnology Applications**
Author(s): Deji Akinwande, Stanford University; Shinichi Yasuda, Bipul Paul, Toshiba Corporation Semiconductor Company; Shinobu Fujita, Toshiba Corporation; Gael Close, Philip Wong, Stanford University

**A3L-C2** 11.40
**Improved Sub-Threshold Slope in RF Vertical MOSFETS Using a Frame Gate Architecture**
Author(s): Mohammad Al Hakim, Takashi Uchino, William Redman White, Peter Ashburn, University of Southampton; Lizhe Tan, Octavian Buiu, Steve Hall, University of Liverpool

**A3L-C3** 12.00
**Improved Analog Performance of Strained Si N-MOSFETs on Thin SiGe Strained Relaxed Buffers**
Author(s): Olayiwola Alatise, Kelvin Kwa, Sarah Olsen, Anthony O'Neill, Newcastle University

**A3L-C4** 12.20
**Novel Wide-Emitter SiGe HBT Technology for RF Power Applications**
Author(s): Katsuyoshi Washio, Central Res Lab, Hitachi, Ltd; Hiromi Shimamoto, Renesas Northern Japan Semiconductor, Inc; Makoto Miura, Katsuya Oda, Central Res Lab, Hitachi, Ltd;

12.50 Lunch

**A4L-A** Pentland
**Joint plenary** V. Manian
Chair(s): Bill Redman-White, NXP/University of Southampton
Robert Henderson, University of Edinburgh

**A4L-A1** 14.10
**Technology Interfacing for Fabless Semiconductor Companies**
Author(s): Vahid Manian, Broadcom

**A5L-A** Fintry
**ESSDERC plenary** T. Hamamoto
Chair(s): Reinout Woltjer, NXP
Roberto Bez, Numonyx

**A5L-A1**
**Overview and Future Challenges of Floating Body Ram**

15.00 **(FBRAM) Technology for 32 nm Technology Node and Beyond**
Author(s): Takeshi Hamamoto, Takashi Ohsawa, Toshiba Corporation

15.40 Coffee break

**A6L-B** **Floating-Gate and Charge-Trap NAND Memories**
Fintry
Chair(s): Tejas Krishhnamohan, Intel Corporation and Stanford University
Barbara De Salvo, CEA-LETI

**A6L-B1** **Impact of the Charge Transport in the Conduction Band on the Retention of Si-Nitride Based Memories**
16.10
Author(s): Elisa Vianello, Francesco Driussi, Pierpaolo Palestri, Antonio Arreghini, David Esseni, Luca Selmi, Università di Udine; Nader Akil, Michiel van Duuren, Dusan Golubovic, NXP-TSMC Res Center Leuven (BE)

**A6L-B2** **16-Gigabit, 8-Level NAND Flash Memory with 51 nm 44-Cell String Technology**
16.30
Author(s): Tae-Kyung Kim, Sungnam Chang, Seungwan Hong, Dong Hyuk Chae, Keonho, Jeong-Hyuk Choi, Samsung Electronics Co Ltd

**A6L-B3** **Si-Nanowire TAHOS (TaN/$Al_2O_3$/$HfO_2$/$SiO_2$/Si) Nonvolatile Memory cell**
16.50
Author(s): Navab Singh, Institute of Microelectronics; J Fu, Institute of Microelectronics and National University of Singapore; B Yang, Institute of Microelectronics; C Zhu, Institute of Microelectronics and National University of Singapore; G Lo, D Kwong, Institute of Microelectronics

**A6L-B4** **On the Role of a HTO/$Al_2O_3$ Bi-Layer Blocking Oxide in Nitride-Trap Non-Volatile Memories**
17.10
Author(s): Marc Bocquet, Gabriel Molas, Luca Perniola, Xavier Garros, Julien Buckley, Marc Gély, Jean-Philippe Colonna, Helen Grampeix, François Martin, Vincent Vidal, Alain Toffoli, Barbara De Salvo, Simon Deleonibus, CEA LETI – MINATEC; Georges Pananakakis, IMEP/MINATEC/CNRS/INPG; Gérard Ghibaudo, IMEP/LAHC

**A6L-B5** **Scaling of Floating Gate Electrode for Sub-40 nm Flash Technologies**
17.30
Author(s): Joeri De Vos, Dirk Wellekens, Ingrid Debusschere, Jan Van Houdt, IMEC; Steven Van Aerde, Pamela Fischer, Peter Zagwijn, ASM

**A6L-C** **Characterisation of Advanced Front-End Materials**
Sidlaw
Chair(s): Henryk Przewlocki, Institute of Electron Technology
Stefan Bengtsson, Chalmers University of Technology

**A6L-C1** **Advantage of La2O3 Gate Dielectric Over $HfO_2$ for Direct Contact and Mobility Improvement**
16.10
Author(s): Kuniyuki Kakushima, Kiichi Tachi, Manabu Adachi, Kouichi Okamoto, Soushi Sato, Jaeyeol Song, Takamasa Kawanago, Parhat Ahmet, Kazuo Tsutsui, Tokyo Institute of Technology; Nobuyuki Sugii, Hitachi, Ltd; Takeo Hattori, Hiroshi Iwai, Tokyo Institute of Technology

**A6L-C2** **Electron Traps at $HfO_2$/$SiO_x$ Interfaces**

16.30
Author(s): Bahman Raeissi, Yangyin Chen, Johan Piscator, Zonghe Lai, Olof Engström, Chalmers University of Technology

**A6L-C3** **Origin of the Flat-Band Voltage (Vfb) Roll-Off Phenomenon in Metal/High-K Gate Stacks**
16.50
Author(s): Gennadi Bersuker, C S Park, H C Wen, Kisik Choi, Sematech; Onise Sharia, Alex Demkov, University of Texas

**A6L-C4** **Impact of Si-Thickness on Interface and Device Properties for Si-Passivated Ge pMOSFETs**
17.10
Author(s): Koen Martens, IMEC/Katholieke Universiteit Leuven; Jerome Mitard, Brice De Jaeger, Marc Meuris, IMEC; Herman Maes, Guido Groeseneken, IMEC/Katholieke Universiteit Leuven; Franco Minucci, Felice Crupi, Universita della Calabria

**AL6-C5** **New Analysis of Heavily Doped Boron and Arsenic in Shallow Junctions by X-Ray Photoelectron Spectroscopy**
17.30
Author(s): Kazuo Tsutsui, Masamitsu Watanabe, Yasumasa Nakagawa, Tokyo Institute of Technology; Toru Matsuda, Musashi Institute of Technology; Tetsuya Yoshida, Meiji University; Eiji Ikenaga, JASRI/Spring-8; Kuniyuki Kakushima, Parhat Ahmet, Tokyo Institute of Technology; Hiroshi Nohira, Takuya Maruizumi, Atsushi Ogura, Meiji University; Musashi Institute of Technology; Takeo Hattori, Horoshi Iwai, Tokyo Institute of Technology

## Wednesday September 17

**B1L-A** **Joint plenary** C. Van Hoof
Pentland
Chair(s): Stephen Hall, University of Liverpool
Peter Ashburn, University of Southampton

**B1L-A1** **Micropower Energy Scavenging**
08.30
Author(s): Paolo Fiorini, Inge Doms, Chris van Hoof, Ruud Vullers, IMEC

**B2L-A** **ESSDERC plenary** D. Antoniadis
Fintry
Chair(s): Athanasis Dimoulas, NCSR Demokritos
Anthony O'Neill, Newcastle University

**B2L-A1** **The Future of High-Performance CMOS: Trends and Requirements**
09.30
Author(s): Ali Khakifirooz, Dimitri Antoniadis, MIT

**B3L-B** **SRAM and Alternative NV Memories**
Fintry
Chair(s): Roberto Bez, Numonyx
Luc Haspeslagh, IMEC

**B3L-B1** **Enhancing Noise Margins of FinFET SRAM by Integrating Vth-Controllable Flexible-Pass-Gates**
10.40
Author(s): Kazuhiko Endo, Shin-Ichi O'Uchi, Yuki Ishikawa, Yongxum Liu, Takashi Matsukawa, Meishoku Masahara, Kunihiro Sakamoto, Junichi Tsukada, Ken-Ichi Ishii, Hiromi Yamauchi, Eiichi Suzuki, National Institute of Advanced Industrial Science and Technology

**B3L-B2** **A Power-Efficient impoved-Stability 6T SRAM Cell in 45 nm Multi-Channel FET Technology**
11.00
Author(s): Olivier Thomas, CEA LETI – MINATEC; Bernard Guillaumot, STMicroelectronics; Thomas Ernst, CEA LETI; Bastien Cousin, Olivier Rozeau, CEA

**B3L-B3** **An Integrated Multi-Physics Approach to the Modeling of a Phase-Change Memory Device**
11.20
Author(s): Stefania Braga, Alessandro Cabrini, Guido Torelli, University of Pavia

**B3L-B4** **On the RESET-SET Transition in Phase Change Memories**
11.40
Giuseppina Puzzilli, Fernanda Irrera, Università di Roma La Sapienza; Paolo Pavan, Luca Larcher, Ankur Arya, Vincenzo Della Marca, Università di Modena e Reggio Emilia; Andrea Padovani, Università di Ferrara; Agostino Pirovano, STMicroelectronics

**B3L-B5** **Low Voltage Ferroelectric FET with Sub-100nm Copolymer P(VDF-TrFE) Gate Dielectric for Non-Volatile 1T Memory**
12.00
Author(s): Giovanni Antonio Salvatore, Didier Bouvet, Igor Stolitchnov, Nava Setter, Adrian Mihai Ionescu, Ecole Polytechnique Fédérale de Lausanne

**B3L-C** **Applied Modelling Techniques**
Sidlaw
Chair(s): An De Keersgieter, IMEC

**B3L-C1** **FinFET Stress Engineering Using 3D Mechanical Stress and 2D Monte Carlo Device Simulation**
10.40
Author(s): Fabian Bufler, Luca Sponton, Axel Erlebach, Synopsys Schweiz GmbH

**B3L-C2** **Deterministic Simulation of SiGe HBTs Based on the Boltzmann**
11.00 **Equation**
Author(s): Sung-Min Hong, Christoph Jungemann, Universität der Bundeswehr

**B3L-C3** **Stress Enhancement Concept on Replacement Gate Technology**
11.20 with Top-Cut Stress Liner for nFETs
Author(s): Shinya Yamakawa, Satoru Mayuzumi, Yasushi Tateshita, Hitoshi Wakabayashi, Ansai Hisaharo, Sony Corporation

**B3L-C4** **TCAD Analysis for Channel Profile Engineering with Carbon Doped Si (Si:C) Layer for Post-32 nm Node Bulk Planar nMOSFETs**
11.40
Author(s): Naoki Kusunoki, Akira Hokazono, Shigeru Kawanaka, Ichiro Mizushima, Hisao Yoshimura, Masaaki Iwai, Fumitomo Matsuoka, Toshiba Corporation Semiconductor Company

**B3L-C5** **A Compact Model for Undoped Symmetric Double-Gate MOSFETs with Schottky-Barrier Source/Drain**
12.00
Author(s): Guo Jun Zhu, Xing Zhou, Teck Seng Lee, Lay Kee Ang, Guan Huei See, Shi Huan Lin, Nanyang Technological University

**B4L-A** Pentland
**Joint plenary** T.Sakurai
Chair(s): TBC

**B4L-A1** 13.50
**Solving Issues of Integrated Circuits by 3D-Stacking Meeting with the Era of Power, Integrity Attackers and NRE Explosion and a Bit of Future**
Author(s): Takayasu Sakurai, University of Tokyo

**B5L-A** Pentland
**Process Stability – Joint Session**
Chair(s): Asen Asenov, University of Glasgow

**B5L-A1** 14.40
**On-Chip Leakage Monitor Circuit to Scan Optimal Reverse Bias Voltage for Adaptive Body-Bias Circuit Under Gate Induced Drain Leakage Effect**
Author(s): Masako Fujii, Hiroaki Suzuki, Hiromi Notani, Hiroshi Makino, Hirofumi Shinohara, Renesas Tech Corp

**B5L-A2** 15.00
**Impact of Strain on LER Variability in bulk MOSFETs**
Author(s): Xingsheng Wang, Scott Roy, Asen Asenov, University of Glasgow

**B5L-A3** 15.20
**On the Stability of Fully Depleted SOI MOSFETs Under Lithography Process Variations**
Author(s): Christian Kampen, Tim Fühner, Alexander Burenkov, Andreas Erdmann, Heiner Ryssel, Fraunhofer Institute of Integrated Systems and Device Technology

**B5L-B** Fintry
**Fully Depleted Devices**
Chair(s): Nadine Collaert, IMEC
Carlos Mazure, SOITEC

**B5L-B1**
**Silicon on Thin BOX (SOTB) CMOS for Ultralow Standby Power with Forward-biasing Performance Booster**
Author(s): Takashi Ishigaki, Ryuta Tsuchiya, Yusuke Morita, Hiroyuki Yoshimoto, Nobuyuki Sugii, Hitachi, Ltd; Toshiaki Iwamatsu, Hidekazu Oda, Yasuo Inoue, Renesas Technology Corp; Tetsu Ohtou, Toshiro Hiramoto, University of Tokyo, Shin'Ichiro Kimura, Hitachi, Ltd

**B5L-B2** 15.00
**Metal Gate Thickness Optimization for MuGFET Performance Improvement**
Author(s): Isabelle Ferain, IMEC/Katholieke Universiteit Leuven; Nadine Collaert, Barry O'Sullivan, Thierry Conard, Mihaela Popovici, Sven Van Elshocht, IMEC; Johan Swerts, ASM Belgium; Malgorzata Jurczak, IMEC; Kristin De Meyer, IMEC/Katholieke Universiteit Leuven

**B5L-B3** 15.20
**FDSOI Devices with Thin BOX and Ground Plane Integration for 32 nm Node and Below**
Author(s): Claire Fenouillet-Béranger, Stephane Denorme, STMicroelectronics; Pierre Perreau, CEA LETI; Christel Buj-Dufournet, Olivier Faynot, François Andrieu, Lucie Tosti, CEA LETI – MINATEC; Sebastien Barnola, Thierry Salvetat, CEA LETI; Xavier Garros, CEA LETI – MINATEC; Mikael Casse, CEA LETI; Fabienne

Allain, CEA LETI – MINATEC; Nicolas Loubet, STMicroelectronics; Loan Pham-Nguyen, STMicroelectronics/IMEP; Emilie Deloffre, STMicroelectronics

**B5L-B4** **Folded Fully Depleted Bulk+ Technology as a Highly W-Scaled Planar Solution**
15.40
Author(s): Gregory Bidal, Nicolas Loubet, Claire Fenouillet-Béranger, Stephane Denorme, STMicroelectronics; Pierre Perreau, CEA LETI; Daniel Chanemougame, Cyrille Laviron, François Leverd, STMicroelectronics; Sebastien Barnola, CEA LETI; R Beneyton, C Duluard, J Chapon, P Gouraud, T Salvetat, M Grosjean, STMicroelectronics

**B5L-C** **Carbon Nanotubes and New Materials**
Sidlaw
Chair(s): Franz Kreupl, Qimonda
Adrian Ionescu, EPFL

**B5L-C1** **Reduction of the Dark-Current in Carbon Nanotube Photo-Detectors**
14.40
Author(s): Mahdi Pourfath, Hans Kosina, Vienna University of Technology; Siegfried Selberherr, Vienna University of Technology/Institute for Microelectronics

**B5L-C2** **Integration of Resistive Switching NiO in Small via Structures from Localized Oxidation of Nickel Metallic Layer**
15.00
Author(s): Lorene Courtade, Christian Turquat, Institut Materiaux Microelectronique et Nanosciences de Provence; Judit Lisoni, Ludovic Goux, Dirk Wouters, Interuniversity MicroElectronics Center; Damien Deleruyelle, Christophe Muller, Institut Materiaux Microelectronique et Nanosciences de Provence

**B5L-C3** **An Analytical Model for Intrinsic Carbon Nanotube FETs**
15.20
Author(s): Lan Wei, Stanford University; David Frank, Leland Chang, IBM Research; Philip Wong, Stanford University

**B5L-C4** **Study of Ferrocene/Silicon Hybrid Memories: Influence of the Chemical Linkers and Device Thermal Stability**
15.40
Author(s): Tiziana Pro, CEA LETI; Julien Buckley, CEA LETI – MINATEC; R Barattin, A Calborean, CEA LETI; Marc Gély, CEA LETI – MINATEC; K Huang, G Delapierre, F Duclairoir, E Jalaguier, P Maldivi, CEA LETI;, Barbara De Salvo, Simon Deleonibus, CEA LETI – MINATEC; Gérard Ghibaudo, IMEP/LAHC

16.00 Coffee break

**B6L-B** **Characterisation of Advanced Devices**
Fintry
Chair(s): Ken Uchida, Tokyo Institute of Technology
Atanasis Dimoulas, NCSR Demokritos

**B6L-B1** **A Mobility Extraction Method for 3D Multichannel Devices**
16.30
Author(s): Thomas Ernst, Cécilia Dupré, CEA LETI; Emilie Bernard, Bernard Guillaumot, Nathalie Vulliet, Philippe Coronel, Thomas Skotnicki, STMicroelectronics; Sorin Cristoloveanu, CNRS/IMEP; Gérard

Ghibaudo, IMEP/LAHC; Simon Deleonibus, CEA LETI – MINATEC

**B6L-B2** **Experimental and Theoretical Analysis of Hole Transport in Uniaxially Strained pMOSFETs**
16.50
Author(s): Karim Huet, University Paris-Sud/CNRS/STMicroelectronics; Maxime Feraille, Denis Rideau, Romain Delamare, STMicroelectronics; Valerie Aubry-Fortuna, CNRS; Moustafa Kasbari, Sylvain Blayac, Ecole des Mines de Saint-Etienne, Centre de Microelectronique de Provence; Christian Rivero, STMicroelectronics Rousset; Arnaud Bournel, University Paris-Sud; Clément Tavernier, STMicroelectronics Crolles; Philippe Dollfus, CNRS; Herve Jaouen, STMicroelectronics Crolles

**B6L-B3** **Influence of Gate Underlap in AM and IM MuGFETs**
17.10
Author(s): Chi-Woo Lee, Aryan Afzalian, Ran Yan, Nima Dehdashti, Jean-Pierre Colinge, Tyndall National Institute, University College Cork; Weize Xiong, Texas Instruments Inc

**B6L-B4** **Extracting Energy Band Offsets on Thin Silicon-on-Insulator MOSFETs**
17.30
Author(s): Jan-Laurens van der Steen, Ray Hueting, MESA, University of Twente; Jurriaan Schmitz, MESA Institute for Nanotechnology, University of Twente

**B6L-C** **Progress in Device Modelling**
Sidlaw
Chair(s): Bernd Meinerzhagen, TU Braunschweig

**B6L-C1** **Revised Analysis of the Mobility and ION Degradation in High-K Gate Stacks: Surface Optical Phonons Vs. Remote Coulomb Scattering**
16.30
Author(s): Paolo Toniutti, Pierpaolo Palestri, David Esseni, Luca Selmi, Università di Udine

**B6L-C2** **Drain Current Improvements in Uniaxially Strained p-MOSFETs: A Multi-Subband Monte Carlo Study**
16.50
Author(s): Francesco Conzatti, Marco De Michielis, David Esseni, Pierpaolo Palestri, Università di Udine

**B6L-C3** **Fully Self-Consistent k.p Solver and Monte Carlo Simulator for Hole Inversion Layers**
17.10
Author(s): Luca Donetti, Francisco Gámiz, Andres Godoy, Noel Rodriguez, University of Granada

**B6L-C4** **Simulation of intravalley Acoustic Phonon Scattering in Silicon Nanowires**
17.30
Author(s) Martin Frey, Aniello Esposito, Andreas Schenk, ETH

## Thursday 18 September

**C1L-A** **Joint plenary** M. Thompson
Pentland
Chair(s): Peter Mole, Intersil

**C1L-A1** **More Than Moore and More Moore in Europe**
08.30

Author(s): Michael Thompson, STMicroelectronics

**C2L-B** **Optical Detectors**
Fintry
Chair(s): Eugenio Cantatore, Eindhoven University of Technology
Ralph Steiner-Vanha, Analog Devices Inc

**C2L-B1** **A Single Photon Detector Implemented in a 130 nm CMOS Imaging Process**
09.30
Author(s): Marek Gersbach, Christiano Niclass, Edoardo Charbon, Ecole Polytechnique Fédérale de Lausanne; Justin Richardson, STMicroelectronics/University of Edinburgh; Robert Henderson, University of Edinburgh; Lindsay Grant, STMicroelectronics

**C2L-B2** **100 kframe/s 8 Bit Monolithic Single-Photon Imagers**
09.50
Author(s): Simone Tisa, Fabrizio Guerrieri, Alberto Tosi, Franco Zappa, Politecnico di Milano

**C2L-B3** **Pure Boron-Doped Photodiodes: a Solution for Radiation Detection in EUV Lithography**
10.10
Author(s): Francesco Sarubbi, Lis Nanver, Tom Scholtes, Delft University of Technology; Stoyan Nihtianov, ASML Netherlands B V; Frank Scholze, Physikalisch-Technische Bundesanstalt

**C2L-C** **Transistor Engineering**
Sidlaw
Chair(s): Simon Deleonibus, CEA LETI
Bich-Yen Nguyen, Soitec

**C2L-C1** **Dual Metal Gate FinFET Integration by Ta/Mo Diffusion Technology for Vt Reduction and Multi-Vt CMOS Application**
09.30
Author(s): Takashi Matsukawa, Kazuhiko Endo, Yongxun Liu, Shin-Ichi O'Uchi, Meishoku Masahara, Yuki Ishikawa, Hiroma Yamauchi, Junichi Tsukada, Ken-Ichi Ishii, Kunihiro Sakamoto, Eiichi Suzuki, National Institute of Advanced Industrial Science and Technology

**C2L-C2** **N-Type VT Tuning by Te Ion Implantation in Moly-Based Metal Gates with High-K Dielectric for Fully Depleted Devices**
09.50
Author(s): Jasmine Pétry, Guillaume Boccardi, Ka Xiong, Markus Müller, Jacob Hooker, NXP-TSMC Research Center; Raghunath Singanamalla, Nadine Collaert, Kristin Demeyer, IMEC

**C2L-C3** **Vacancy Engineering for Highly Activated 'Diffusionless' Boron Doping in Bulk Silicon**
10.10
Author(s): Nick Bennett, Nick Cowern, Newcastle University; Silke Paul, Wilfried Lerch, Mattson; Hamid Kheyrandish, CSMA-MATS; Andy Smith, Russell Gwilliam, Brian Sealy, University of Surrey

**C2L-C4** **Process-Induced SOI Strain via Sacrificial Ge-Si**
10.30
Author(s): Daniel Connelly, Paul Clifton, Acorn Technologies

10.50 Coffee break

**C3L- B** **Sensors and MEMS**
Fintry

Chair(s): Carlotta Guiducci, Deis – University of Bologna
Roland Thewes, Qimonda

**C3L-B1** **Supersensitive Si-Integrated Tin Oxide Nanowire-Sensors for Gas Detection**
11.20
Author(s): Anton Koeck, Thomas Maier, Alexandra Tischner, Austrian Research Centers GmbH ARC; Christian Edtmaier, Vienna University of Technology; Christian Gspan, Gerald Kothleitner, Graz Centre for Electron Microscopy

**C3L-B2** **Double Gate Movable Body Micro-Electro-Mechanical FET as Hysteretic Switch: Application to Data Transmission Systems**
11.40
Author(s): Daniel Grogg, Cedric Meinen, Dimitrios Tsamados, Huseyin Cumhur Tekin, Maher Kayal, Adrian Mihai Ionescu, Ecole Polytechnique Fédérale de Lausanne

**C3L-B3** **Wireless Driven EWOD Technology for a MEMS Pond Skater**
12.00
Author(s): Yifan Li, SMC, University of Edinburgh; Yoshio Mita, Masanori Kubota, University of Tokyo; William Parkes, Les Haworth, Brian Flynn, Jonathan Terry, Tong-Boon Tang, Alec Ruthven, Stewart Smith, Anthony Walton, University of Edinburgh;

**C3L-C** **Emerging Silicon Devices**
Sidlaw
Chair(s): Olof Engstrom, Chalmers University of Technology
Ryoichi Ishihara, Tu Delft (NL)

**C3L-C1** **Non-Hysteretic punchthrough Impact Ionization MOS (PIMOS)** Transistor: Application to Abrupt Inverter and NDR Circuits
11.20
Author(s): Vincent Pott, Kirsten Moselund, Adrian Mihai Ionescu, Ecole Polytechnique Fédérale de Lausanne

**C3L-C2** **Enhanced Tunnel Conductance Due to QCA cotunneling Processes Observed for Silicon Serial Triple Quantum Dots**
11.40
Author(s): Gento Yamahata, Ken Uchida, Shunri Oda, Tokyo Institute of Technology; Yoshishige Tsuchiya, Hiroshi Mizuta, University of Southampton

**C3L-C3** **CMOS Compitable Gate-All-Around Vertical Silicon-Nanowire MOSFETs**
12.00
Author(s): B Yang, K D Buddharaju, S H G Teo, J Fu, Navab Singh, G Q Lo, D Kwong, Institute of Microelectronics

**C3L-C4** **Detection of Single-Charge Polarisation in Silicon Double Quantum Dots by Using Serially-Connected Multiple Single-Electron Transistors**
12.20
Author(s): Yoshishige Tsuchiya, University of Southampton; Shunri Oda, Yoshiyuki Kawata, Tokyo Institute of Technology; Hiroshi Mizuta, University of Southampton

12.40 Lunch

**C4L-A** **Joint plenary** V. Subramanian
Pentland
Chair(s): Roland Thewes, Qimonda
Ralf Brederlow, Texas Instruments Deutschland GmbH

**C4L-A1** 14.10 — **Printed Electronics for Low-Cost Electronic Systems: Technology Status and Application Development**
Author(s): Vivek Subramanian, Josephine Chang, Alejandro de la Fuente Vornbrock, Daniel Huang, Lakshmi Jagannathan, Frank Liao, Brian Mattis, Steve Molesa, David Redinger, Daniel Soltman, Steven Volkman, Qintao Zhang, University of California, Berkeley

**C5L-A** Fintry — **ESSDERC plenary** K. Saraswat
Chair(s): Atanasis Dimoulas, NCSR Demokritos
Asen Asenov, University of Glasgow

**C5L-A1** — **High Mobility Ge and III-V Materials and Novel Device 15.00 Structures for High Performance Nanoscale MOSFETS**
Author(s): Tejas Krishnamohan, Stanford University and Intel Corp; Krishna Saraswat, Stanford University

15.40 Coffee break

**C6L-B** Fintry — **Source and Drain Engineering**
Chair(s): Giuseppe Iannaecone, University of Pisa
Emmanuel Dubois, IEMN

**C6L-B1** 16.10 — **A Study on Aggressive Proximity of Embedded SiGe with Comprehensive SDE Engineering for 32 nm-Node High-Performance pMOSFET Technology**
Author(s): Hiroki Okamoto, N Yasutake, N Kusunoki, K Adachi, H Itokawa, K Miyano, T Ishida, A Hokazonao, S Kawanaka, Ichiro Mizushima, A Azuma, Y Toyoshima

**C6L-B2** 16.30 — **Comprehensive Study of S/D Engineering for 32 nm Node CMOS in Direct Silicon Bonded (DSB) Technology**
Author(s): Nobuaki Yasutake, A Nomachi, H Itokawa, T Morooka, L Zhang, T Fukushima, H Harakawa, Ichiro Mizushima, A Azuma, Y Toyosihma

**C6L-B3** 16.50 — **Improved Fin Width Scaling in Fully-Depleted FinFETs by Source- Drain Implant Optimization**
Author(s): Ray Duffy, Mark Van Dal, Bartek Pawlak, NXP-TSMC Research Center; Nadine Collaert, Liesbeth Witters, Rita Rooyackers, IMEC; Monja Kaiser, Robbert Weemaes, Philips Research Laboratories Eindhoven; Malgorzata Jurczak, IMEC; Robert Lander, NXP-TSMC Research Center

**C6L-B4** 17.10 — **N-MOSFETs with Inversion-Layer Source/Drain Extensions Formed by Cesium Segregation at SiO2/Si Interfaces**
Author(s): Kenji Kimoto, MIRAI-ASET; Tetsuya Tada, Toshihiko Kanayama, MIRAI-ASRC, National Institute of Advanced Industrial Science and Technology

# ESSDERC workshops

## WS 1 CMOS Variability Research in Europe: From Atomic Scale to Circuits and Systems

The increasing variability in CMOS transistor characteristics has become a major challenge to scaling and integration. Statistical variability related to the fundamental discreteness of charge and matter, which cannot be eliminated by tighter process control, is becoming the major component of CMOS variability. The increasing device variability demands fundamental changes in the way that future integrated circuits and systems are designed. Strong links must be established between circuit design, system design and fundamental device technology to allow circuits and systems to accommodate the individual behaviour of every transistor on a chip. Design paradigms must change to accommodate the increasing variability. This workshop presents the status of CMOS variability related research in Europe conducted in three European and two national projects, including:

**NANOSIL** Silicon-based nanostructures and nanodevices for long-term nanoelectronics applications (EU FP7)
**PULLNANO** Pulling the limits of nanoCMOS Electronics (EU FP6)-
**REALITY** Reliable and variability tolerant system-on-a-chip design in More-Moore technologies (EU FP7)-
**NanoCMOS** Meeting the design challenges of nanoCMOS electronics (UK EPSRC)-
**NanoMat** Meeting the material challenges of nanoCMOS electronics (UK EPSRC)-

The workshop covers a broad range of technology, devices, and design aspects of the CMOS variability from atomic scale to circuit and system level. The keynote speaker, Prof. Toshiro Hiramoto from Tokyo University, will introduce the subject and will present the concerted research effort, supported by the MIRAI Project in Japan, in characterising and understanding the sources of statistical CMOS variability.

### Agenda

| | |
|---|---|
| 09.00 | **Welcome and introduction** A. Ionescu, EPFL, Switzerland |
| 09.10 | **Measuring and Understanding Device Variability** Keynote, T. Hiramoto, Tokyo University (MIRAI) |
| 09.40 | **Link Between 'Ab Initio' Material Simulation and Variability** A. Shuger, UCL (NanoMAT) |
| 10.10 | **Simulation of Statistical Variability Introduced by Discreteness of Charge and Matter** A. Asenov, University of Glasgow (NanoMAT) |
| 10.40 | Coffee break |
| 11.00 | **Measuring and Simulation of STMicroelectronics/Device Variability at 45 nm Technology Generation** A. Cathignol, IMEP |

11.30 **Measurement and Simulation of Statistical Variability in FinFETS** A. Mercha, IMEC (PULLNANO)

12.00 **Variability in Novel Device Architectures** G. Iannaccone, IU.NET (NANOSIL)

12.30 Lunch

13.30 **Reliable and Variability-Tolerant System-on-Chip Design Strategies** B. Dierickx & M. Miranda, IMEC (REALITY)

14.00 **Grid Technology to Support Statistical Device and Circuit Simulation** S. Roy, University of Glasgow (NanoCMOS)

14.30 **Impact of Variability on Multicore Processor Architectures** S. Furber, Manchester University (NanoCMOS)

15.00 **Hardware-Software Interactions in Variability and Reliability Aware Design** L. Benini, University of Bologna (REALITY)

15.30 Coffee break

16.00 **Brainstorming Session: Practical Solution for Variability Resistant Devices, Circuits and Systems** A. Shluger, A. Asenov, G. Ghibaudo, S. Furber, B. Dierickx, industry representatives

17.00 End of workshop

## WS 2 Electronic cubes: a More-than-Moore platform for Wireless Sensor Nodes exploiting the 3rd Dimension

### Agenda

09.00 **Opening and Short Introduction** A. Ionescu, EPFL, Switzerland

09.15 **Morphic Architectures: Atomic-Level Limits (10 μm cube)** (KEYNOTE) Ralph Cavin, Semiconductor Research Corporation, Reasearch Triangle Park, USA

09.45 **Overview of Integrated Project e-CUBES** Werner Weber, Infineon, Germany

10.15 Coffee break

10.45 **e-CUBES 3D Integration Technologies** Thierry Hilt, CEA, France

11.15 **e-CUBES Functional Blocks for 3D Integration** TBD

11.45 **Overview of MINAmI Project: Towards Ambient Intelligence for Everyday Life** (INVITED) Pascal Ancey, Industry Representatives STMicroelectronics, France

12.15 Lunch

14.00 **Energy Scavenging Research at the University of Southampton** (INVITED) Stephen Beeby, University of Southampton, UK

14.30 **Overview of Project NANOPACK** (INVITED) Afshin Ziaei, Thales, France

15.00 **Wireless Sensor Networks for Space** TBD, EPFL, Switzerland

15.30 End of workshop

## WS 3 Workshop on Germanium and III-V MOS Technology

The time when technology-driven dimensional scaling could provide simultaneously high-density/low cost and high performance circuits is over. Further scaling does not guarantee performance benefits. From now on, novel device architectures and new materials may be necessary to obtain the required performance. In fact, Hf-based dielectric/metal gate combinations have replaced the long standing $SiO_2$/polysilicon in the gate of transistors. The new gates are already in production for the 45 nm CMOS since the end of 2007 by leading ICs manufacturer. What is next? Some people believe that new high mobility channels such as germanium and III-V compounds may be needed for future device generations.

In this workshop experts from academia, technology development laboratories and semiconductor manufacturers will come together to discuss the challenges toward a viable high mobility MOS technology. The experts will describe large scale initiatives in the US, Asia and Europe and they will introduce the main issues which will be subsequently debated in two panel discussions.

In the first morning session we will address issues related to gate dielectric and device architecture and performance. At the end, during the panel discussion we will try to answer a few difficult questions. Is it feasible to develop a complementary MOS technology which will be based entirely on Germanium? The answer to this question is not easy at the present time. We can only say that Ge CMOS is highly desirable because it simplifies processing. The main obstacle is that Ge nMOSFETs do not work as expected and we do not know why. Is this problem related to materials and/or device processing or is it of more fundamental nature related to the semiconductor itself? In the case of III-V MOSFETs, the problems are even more difficult to solve. The consensus is that a high density of defect states, probably near midgap, pin the Fermi level, thus inhibiting inversion in GaAs.

Which is the best way to passivate the GaAs surface? Which is the best device architecture and operation mode? Is it better to go for surface inversion-type with implanted S/D or buried channel implant-free devices? Is InGaAs channel better than GaAs and why?

While high mobility channels show advantage over Si in discrete long channel research devices, the situation becomes unclear when dimensions shrink. Will mobility retain high values or will it degrade as in the case of Si nanoscaled devices? More importantly, is mobility a relevant physical quantity at nanoscale dimensions or perhaps quasi-ballistic transport sets new rules for the on-state current and performance in general? Will the off-state current be under control especially for Ge devices which are expected to suffer from band-to-band tunneling?

During the second session in the afternoon and in the panel discussion at the end we will address integration issues including heteroepitaxy and engineered substrates, self-aligned processing, junctions and contacts. As it looks right

now, Ge performs well for pMOS only while III-V compounds are good for nMOS, therefore Ge and III-V compounds are not competing materials; rather, they could complement each other to form a dual-channel CMOS, provided that a good co-integration scheme can be found. Which will be the best starting substrate, plain Si or GeOI? Do we have good solutions for the problems associated with heteroepitaxial growth of III-V compounds on Ge or Si? Is dual-channel Ge/III-V better than Ge/s-Si counterpart? Do we know how to process III-Vs in a self-aligned way to guarantee scaling to very small dimensions? After all, is high mobility dual-channel CMOS scalable and manufacturable so that it could be a viable technology for volume production?

**Session 1: Gate materials and devices**

### Agenda

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|---|---|
| 09.00 | **Overview of Advanced High Mobility/High Velocity Research Devices** D. Antoniadis, MIT |
| 09.20 | **Device Architecture and Processing for III-V MOS Technology** M. Rodwell, UCSB |
| 09.40 | **Devices for High Performance CMOS** S. Takagi, University of Tokyo |
| 10.00 | Coffee break |
| 10.20 | **Nanoscale Ge and III-V FETs** T. Krishnamohan, Intel/Stanford University |
| 10.40 | **GaGdO and Al2O3- Passivated II-V MOSFETs** M. Hong Nat, Tsing Hua University |
| 11.00 | **A -Si-Passivated III-V MOSFETs** J. Fompeyrine, IBM-Zurich Res. Lab |
| 11.20 | **Panel Discussion 1 Speakers Session 1: Moderator A. Dimoulas** |
| 12.00 | Lunch |

**Session 2: Substrates and Integration**

### Agenda

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|---|---|
| 13.30 | **Ge-on-Nothing for Ultrathin Ge Microelectronics Film Integration** T. Skotnicki, ST |
| 13.50 | **GeOI/sSOI for Co-Inegration of s-Ge pMOS with s-Si nMOS** L. Clavelier, CEA-LETI |
| 14.10 | **Sub-100 nm Ge pMOS Using Si-Compatible Process Flow** M. Heyns IMEC |
| 14.30 | **Co-Integration of Ge pMOS with III-V nMOS for Heterogeneous** |
| 14.50 | **Process Modules for Implant-Free III-V MOSFETs** I. Thayne U. |

Glasgow

15.10 **Panel Discussion 2 Speakers Session 2: Moderator A. Dimoulas**

15.50 End of workshop

## WS 4 MOS-AK: Towards Nano Compact Modeling Compact Modeling and Transistor Level Optimization in Analog Designs for Nano CMOS/SOI Technologies

MOS-AK Workshop on compact modelling, organised for sixth subsequent time as an integral part of the ESSDERC/ESSCIRC conference, aims to strengthen a network and discussion forum among experts in the field, create an open platform for information exchange related to compact/spice modelling, bring people in the compact modelling field together, as well as obtain feedback from technology developers, circuit designers, and CAD tool vendors. The topics cover all important aspects of compact model development, implementation, deployment and standardisation within the main theme - compact models for mainstream CMOS/SOI circuit simulation. The specific workshop goal will be to classify the most important directions for the future development of the compact models and to clearly identify areas that need further research. This workshop is designed for device process engineers (CMOS, SOI, BiCMOS, SiGe) who are interested in device modelling; ICs designers (RF/IF/analogue/mixed-Signal/SoC) and those starting in that area as well as device characterisation, modelling and parameter extraction engineers. The content will be beneficial for anyone who needs to learn what is really behind IC simulation in modern device models. The technical program of MOS-AK workshop consists of one day of tutorials given by noted academic and industry experts, also a posters session is foreseen which will be dedicated but not limited to the VHDL-AMS/Verilog-A model standardisation: http://www.mos-ak.org/edinburgh

**Transistor Level Optimization in Analog Designs** David M. Binkley, UNC Charlotte

**Aspects of high-frequency modelling of MOSFETs with EKV3** Matthias Bucher, TUC

**Transistor Modeling for Low-Power and RF IC Designs** Christian Enz, CSEM

**Compact modeling techniques in thin-film SOI MOSFETs** Benjamin Iniguez, URV

**High-level modelling and performance optimisation of mixed-technology energy harvester systems** Tom J. Kazmierski, University of Southampton

**LDMOS Model Benchmark for HiSIM LDMOS, MM20 and BSIM3v3 Sub-circuit** Ehrenfried Seebacher, austriamicrosystems

**Compact model challenges of 65nm RF-CMOS technology** Sadayuki Yoshitomi, TOSHIBA

### Agenda

09.00 Oral presentations

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|---|---|
| 10.00 | Coffee break |
| 10.30 | Oral presentations |
| 11.30 | Posters |
| 12.00 | Lunch |
| 13.00 | Oral presentations |
| 14.30 | Coffee break |
| 15.00 | Oral presentations |
| 16.00 | End of workshop |

## WS 5 BIES: Brain-Inspired Electronic Systems

Significant research has focused on the development of neural networks (NNs) models that can be implemented in hardware and used to inspire new techniques for real time computations.

However, there exist several fundamental bottlenecks that restrict the progress towards biological scale networks in hardware: power consumption, compactness of neuron cells and interconnect, off vs. on chip training, etc. A workshop, held on 19 September at ESSCIRC/ESSDERC08, has the aim of bringing together researchers to discuss issues related to the development of novel hardware platforms for Brain-Inspired Electronic Systems. The workshop will provide an opportunity for researchers focusing on various aspects of such systems, such as hardware implementation of spiking neurons and the associated networks, to discuss and compare different approaches to the realisation of large-scale platforms. In particular, we would like the session to draw on the expertise of researchers to provide a discussion platform on many issues related to this domain. Also the workshop will provide an opportunity to discuss applications of brain-inspired electronic systems: for example, fault tolerant computational systems.

### Agenda

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|---|---|
| 09.00 | **Introduction and Overview: Brain-Inspired Electronic Systems and the Electronics Knowledge Transfer Network** D. Dearing, Technology Business Manager, Electronics-KTN, UK; W. Luk, Imperial College London, UK |
| 10.00 | **Coffee, posters and networking:** interested delegates are encouraged to present a poster to promote their research |
| 10.45 | **An overview of neuromorphic circuit research at ETH** Giacomo Indiveri, ETHZ, Switzerland |
| 11.15 | **Circuit design for biologically plausible neural models** Piotr Dudek, University of Manchester, UK |
| 11.55 | **Neuromorphic Computation and Control: Bio-Inspired Systems** Leena Patel/Alan Murray, University of Edinburgh, UK |

12.15 Networking lunch

13.30 **Abstracting Both Architecture and Time: The SpiNNaker Neuromimetic Modelling Platform** A. Rast, S. Furber, D. Lester, S. Temple, L. Plana, E. Painkras, M. Khan, J. Wu, Y. Shi, S. Yang and X. Jin, University of Manchester, UK

14.00 **EMBRACE: A Programmable Hardware Platform for Spiking Neural Networks** S. Hall (University of Liverpool), L. McDaid, J. Harkin (Ulster), P. Dudek (Manchester) and L. Smith(Sterling)

14.30 **Workshop breakout session** facilitated by partner organisations and aimed at identifying themes and research projects including those of use to industry

15.30 **Feedback session and discussion** – nominated speakers from each of the workgroups present the outcomes; followed by open discussion

16.00 Coffee

16.15 **Summary and follow-up** Daniel Dearing, eKTN

Networking and close

## WS 6 Si-based Nanodevices for ultimate CMOS and beyond-CMOS

This workshop aims to establish a discussion forum in the field of nanoelectronics devices. It is supported by the SINANO Institute, which is a new European entity founded by the main laboratories of the European academic community working in this field, and by the European Network of Excellence NANOSIL devoted to Silicon-based Nanodevices funded by the European Commission for the 7th Framework Programme.

Over the next quarter-century, considerable challenges exist to push the limits of silicon integration down to nanometric dimensions and to enhance device performance in order to meet the ever increasing demands of communication and computing. The aim of the workshop is to present the status and trends of CMOS and beyond-CMOS nanodevices for terascale ICs.

9.00 **New Channel Materials for Ultimate CMOS** Siegfried Mantl, Institut für Bio- und Nanosysteme, Forschungszentrum Juelich

9.30 **Innovative Device Architectures Nanoscale CMOS** Nadine Collaert, IMEC

10.00 Refreshment break

10.30 **Comparative Analysis of Stress-Induced Performance Enhancement in NMOS and PMOS Transistors** David Esseni, Udine University

11.00 **Characterisation Methods for Nanodevices** Sorin Cristoloveanu, IMEP

11.30 **Emerging Nanotechnology for Integration of Nanostructures in Nanoelectronic Devices** Thierry Baron, LTM

12.00 Lunch

13.30 **Small Slope Switches** Adrian Ionescu, EPFL

14.00 **3D Multichannels and Stacked Nanowires Technologies** Thomas Ernst, LETI

14.30 **Carbon Nanotube – Silicon Heterojunctions for Nanoelectronics and Nanosensors** Jimmy Xu, Brown University

15.00 **Atomic Functionalities in Silicon Devices: Go Beyond the FET by Using Single Dopants and Artificial Silicon Atoms** Marc Sanquer, INAC

15.30 End of workshop

# ESSDERC fringe

The Edinburgh fringe will be held in the exhibition, which is situated n the Cromdale Hall. This session will take place during the afternoon coffee break on Tuesday 16 September 2008. Please refer to the timetable (p6) for further details. Presenters will also be on hand to discuss their posters outside this timeslot by prior arrangement. Please come to the registration desk to arrange an alternative session time.

**P1** **A Micromachined Three-Axis Acceleration Sensor for the Measurement of Heart Wall Motion**
Craig Lowrie, Heriot Watt University, UK

**P2** **On the Design of an Integrated Monolithic 3-Axis Piezoresistive Accelerometer on SOI**
Dr Aboubacar Chaehoi, Institute for System Level Integration, UK

**P3** **Characterization of Binary Oxide Thin Films Regarding the Resistive Switching Effect for the Application in Future High Density Non-Volatile Memories**
Dr Carsten Kuegeler, Centre of Nanoelectronic Systems for Information Technology, Germany

**P4** **Review of the Development of Microscale Magnetic Components for DC-DC Power Converters**
Dr David Flynn, Heriot Watt Uiversity, UK

**P5** **Analysis of the Band-to-Band Tunneling Effect in 65 nm nFETs**
Dr Emmanuel Torres-Rios, INAOE, Mexico

**P6** **Photoelectric Methods to Determine Distributions of Parameter Values over the Gate Area of MOS Devices**
Dr Krzysztof Piskorski, Institute of Electron Technology, Poland

**P7** **Device Process Simulation for EEPROM Cell: Well Optimization for HV Devices**
DipL-Ing Gerard Dubois, Altissemiconductor, France

**P8** **Confined and Guided Catalytic Growth of Crystalline Silicon Films on a Dielectric Substrate**
Miss Aurélie Lecestre, IEMN-UMR CNRS/STMicroelctronics, France

**P9** **Postponing SoC Death**
Mr Ahmed AbdelHamid, Technology Aware Design, Belgium

**P10** **Statistical Simulations of High-K-Based Non-Volatile Memory Devices**
Mr Andrea Padovani, Universita di Ferrara/IU.NET, Italy

**P11** **Impact of the Field Induced Polarization Space-Charge on the Characteristics of AlGaN/GaN HEMT: Self-Consistent Simulation Study**
Mr Daniel Balaz, University of Glasgow, UK

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|---|---|
| **P12** | **Charge Trapping Properties of Sputtered Hafnium Oxide Films on Silicon Dio**xide<br>Mr Emanuele Verrelli, National Technical University of Athens, Greece |
| **P13** | **Field-plate LDMOS Devices for RF Applications**<br>Mr I Cortes, LAAS-CNRS; Universite de Toulouse, France |
| **P14** | **Interfacing Continuous and Particular Ion Transport Techniques in Nano-Bio Electronic Simulations**<br>Mr Iain Moore, University of Glasgow |
| **P15** | **Layout Dependency of PMOS off Current Degradation due to Off-State Stress**<br>Mr Jae Seo, Samsung Electronics, Korea |
| **P16** | **BTI and Dielectric Breakdown in High-k Gated NMOS Transistors Studied using DC and Fast Measurements**<br>Mr Juan Boix, Universitat Autonoma di Barcelona, Spain |
| **P17** | **Study of Apparent Ballistic Magnetoresistance Mobility in Nanometer Scale MOSFETs**<br>Mr Karim Huet, Universite Paris Sud, CNRS/STMicroelectronics, France |
| **P18** | **Impact of Oxide Progressive Soft Breakdown on MOS Devices Operation: Experiment and Modeling**<br>Mr Louis Gerrer, IMEP-LAHC, France |
| **P19** | **Suspended Gate Silicon Nanodot Memory**<br>Mr Mario Garcia-Remirez, University of Southampton, UK |
| **P20** | **High quality Schottky Contacts for Limiting Leakage Currents in Ge Based Schottky Barrier MOSFETs**<br>Mr Muhammad Husain, University of Southampton, UK |
| **P21** | **Investigation of Strain Profile Optimization in Gate-All-Around Suspended Silicon Nanowire FET**<br>Mr Mohammad Najmzadeh, Swill Federal Institute of Technology in Lausanne (EPFL), Switzerland |
| **P22** | **Fabrication of Three-Dimensional Inverters Using the u-Czochralski**<br>Mr Mohammad Tajari Mofrad, Delft University of Technology, Netherlands |
| **P23** | **Numerical Simulation of Quasi-Ballistic Transport in Fully-Depleted SOI and Double-Gate MOSFETs: Application to the Analysis of Circuit Performances**<br>Mr Sébastien Martinie, CEA-LETI MINATEC/IM2NP-CNRS, UMR CNRS 6242 |
| **P24** | **An Axonal Delay Scheme for Spiking Neural Networks**<br>Mr Thomas Dowrick, University of Liverpool, UK |
| **P25** | **SWCNT-MWCNT Crossed Junction by Two-Step** |

**Dielectrophoresis**
Ms Anupama Arun, Nanolab, EPFL, Switzerland

**P26** **From Process to Device: Modelling Ultra-shallow Sb Implants in Strained Silicon**
Ms Yan Lai, Tyndall National Institute, Ireland

**P27** **An Improved Self-consistent Method and Hole Mobility in Ge and GaAs Bulk PMOSFET**
Ms Yan Zhang, University of Massachusetts, USA

**P28** **Positive Charge Trapping Induced by Plasma Charging Damage in NMOS Transistors**
DipL-Ing Sebastian Sommer, Fraunhofer Institut fur Mikroelektronische Schaltungen und Systeme Duisburg, Germany

**P29** **A Proposed Wide Input Linear Range OTA Circuit**
Mr Saad Hasan, University of Liverpool, UK

**P30** **High Efficiency Synchronous Buck Converter using optimised Split-Gate RSO MOSFET**
Mr Chin Tong, University of Warwick, UK

**P31** **Full 3D Real-Space NEGF Simulation of Transport and Magnetotransport in Si-Nanowire FETs**
Mr Claudio Buran, IMEP-LAHC MINATEC, France

**P32** **A High Output Impedance Current Source for Wideband Bio-Impedance Measurements**
Mr Hongwei Hong, University College London, UK

**P33** **Advanced GeOI structures: from Material Properties to High Performance pMOSFETS**
Mr Willliam Van Den Daele, IMEP-LAHC Grenoble – INP MINATEC Grenoble, France

**P34** **Stem Cell Studies Using Micro and Nanostructures**
Mr Aamer Shabbir, Heriot Watt University, UK

**P35** **Micro-Peltier Devices for BioMEMS Applications**
Miss Alice Daniels, Heriot Watt University

**P36** **DNA Nanotechnology Based Biosensors for Rapid Disease Diagnostics**
Wenxing Wang, Heriot Watt University, UK

**P37** **Stochastic Piecewise Modelling of Post-BD Gate Current Oriented to Circuit Design**
Mr Javier Martin-Martinez, Universitat Autonoma di Barcelona, Spain/IMEC, Belgium

**P38** **Operation and Electrical Quenching of Electroluminescence in Multicolor Eu Doped Metal-Oxide-Silicon Light-Emitting Device**
Stanislav Tyagulskiy, Lashkaryov Institute of Semiconductor Physics, National Academy of Sciences of Ukraine

# Notes