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Welcome to ESSCIRC 2008

The European Solid-State Circuits Conference (ESSCIRC) and the European Solid-State Device Research Conference (ESSDERC) are recognised as the premier events in the European microelectronics calendar, with long-established traditions of high-quality presentations covering major aspects of solid-state systems and circuits down to technology and devices. Since 2002 the ESSCIRC and ESSDERC conferences have been organised jointly in recognition of the benefits arising from interaction between the two communities and from the opportunities to participate in presentations from the partner community. Specialists from both communities are able to share perspectives in creating highly complex, and high-precision systems and circuits within the opportunities and constraints of the latest technological advances.

Some 270 high-quality submissions were received for the 34th ESSCIRC conference, from contributors in industry and academia in 27 countries. The global impact of the conference is clearly evident, with 144 papers coming from Europe, 90 from the Asia-Pacific region and 34 from the Americas. About 25% of the submissions came from industry, although with a higher success rate in the reviews.

The difficult task of selecting papers for presentation at the conference was the responsibility of the Technical Programme Committee (TPC), which is made up of 85 experts from industry and academia around the world. After a rigorous review and voting procedure, the TPC selected 111 papers for oral presentation. Papers are organised in three parallel tracks, with the aim of maximising choice for delegates between specialist areas, with three sessions held jointly with the ESSDERC programme.

In addition to the contributed papers, the programme has a number of invited plenary papers from internationally recognised technical leaders, addressing subjects of topical interest and debate. Six plenary talks are on arange of subjects important to both the circuit design and the device research communities. These presentations cover technology interfacing for fabless design companies, research for the 22 nm node, the European position beyond Moore's law, flexible electronics, 3D integration and energy

scavenging. A further three plenary papers deal with subjects specific to the ESSCIRC community, covering ultra low-power biomedical design, the state of the art in audio integration, and SOI design for high-performance processors.

In addition to the main conference presentations, there is a comprehensive tutorial programme on the day before, with advanced material for the radio-frequency specialist and more broad and accessible coverage of PLLs and filters for the working engineer. At the end of the conference we also have several workshops that deal in depth with issues relating to technology and design.

We would like to acknowledge the efforts of all of those who have contributed to the excellent scientific programme for ESSCIRC 2008. First, thanks go to all of the authors for submitting their research. Second, we would like to express our gratitude to the members of the TPC for their dedication and commitment in undertaking the reviews and making the final selection that determines the success of the conference. Particular thanks go to the conference secretariat for handling all aspects of this complex event with great competence and efficiency, and for their tireless efforts and dedication.

We look forward to seeing colleagues old and new at the conference this year. We wish all a successful and rewarding time in the excellent scientific programme, and we encourage all to join in the opportunities to develop new contacts as well as renew old ones in the many social activities while staying with us in the beautiful and ancient city of Edinburgh.

William Redman-White
ESSCIRC 2008
Technical Programme Committee chair

Anthony Walton
ESSCIRC 2008
General chair

About the IOP

The Institute of Physics is a scientific membership organisation devoted to increasing the understanding and application of physics. It has an extensive worldwide membership (currently around 35 000) and is a leading communicator of physics with all audiences, from specialists through government to the general public. Its publishing company, IOP Publishing, is a world leader in scientific publishing and the electronic dissemination of physics.

For further information about individual membership or how your company can take advantage of the many benefits of the Corporate Affiliates Network, visit us at our stand during the exhibition at ESSDERC-ESSCIRC 2008, or go to our website, **www.iop.org**. Alternatively, contact:

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Images
ESSCIRC

For further information, visit **www.esscirc2008.org**.

Contents

Timetable

Tutorials

Monday 15 September 2008

Filter Design
Kilsyth Room

08.30	**Filter Theory**
10.00	**Tuning and Reconfiguration for Analog Filters**
11.00	**Discrete Time Including Digital Filters**
12.15	**Question-and-answer session**
12.30	Close

PLL Design
Kilsyth Room

13.30	**The PLL Loop**
15.30	**Example 1: The Radio Synthesiser**
16.00	**Example 2: Clock Recovery from a Pseudo Random Bit Stream**
16.30	**Example 3: Digital PLL for Clock Generation**
17.00	**Question-and-answer session**
17.15	Close

All you want to know about RF CMOS – 1 GHz to 0.1 THz
Tinto Room (all day)

09.00	**Making Measurements on Chip at 50–100 GHz**
09.50	**Construction, Modelling and Characterisation of Passives on Silicon for RF and Millimetre-Wave Applications**
10.40	Coffee break
11.00	**RF Modelling of MOS Transistors for 0.1 THz Operation**
11.50	**RF Circuits for UWB, 3 GHz to 10 GHz**
12.20	Lunch
13.30	**Design of Amplifiers and Mixers in Baseline CMOS**

	Technology
14.00	**Millimeter Wave Design in Bulk and SOI CMOS**
14.30	**RF Assembly and Packaging – Ongoing System Integration**
15.20	Coffee break
15.45	**RF Radio Architectures/System Design for CMOS Applications**
16.35	**Question-and-answer session**

Tuesday 16 September 2008

08.50	**Introduction** Pentland
09.00–09.40	**Joint plenary talk** R. Chau, Pentland
09.50–10.50	**Process Variability and Yield** Joint session, Pentland **Power Converters** Tinto **Temperature and Gas Sensors** Moorfoot **Delay-Locked Loops** Kilsyth
10.50–11.20	Coffee break
11.20–12.50	**RF Building Block** Tinto **Unconventional Image Sensors and Circuits** Moorfoot **On-Chip Digital Monitors and Regulators** Kilsyth
12.50–14.10	Lunch
14.10–14.50	**Joint plenary 2** V. Manian, Pentland
15.00–15.40	**ESSCIRC plenary 1** T. Denison, Pentland
15.40–16.10	Coffee break
16.10–17.50	**Transceivers and Tuners** Tinto **High-Speed Data Links** Moorfoot **Low Power Processors and Memory** Kilsyth
18.30	**Welcome reception, including whisky tasting** Cromdale Hall

Wednesday 17 September 2008

08.30–09.10	**Joint plenary 3** C. Van Hoof, Pentland
09.30–10.10	**ESSDERC plenary 2** Y. Hagihara, Pentland
10.10–10.40	Coffee break
10.40–12.20	**Oversampled Data Converters** Tinto **Memory Design Techniques** Moorfoot **60GHz and Beyond** Kilsyth

13.50–14.30	**Joint plenary 4** T. Sakurai, Pentland
14.40–16.00	**Process Stability** Joint session, Pentland **Nyquist Rate Data Converters** Tinto **Low Power SRAM** Moorfoot **Circuit Techniques for UWB** Kilsyth
16.00–16.30	Coffee break
16.30–17.50	**Amplifiers** Tinto **Components in High Frequency Circuits** Moorfoot **UWB TX Synthesisers** Kilsyth
19.00	**Conference dinner** Murrayfield Stadium

Thursday 18 September 2008

08.30–09.10	**Joint plenary 5** M. Thompson, Pentland
09.30–10.50	**Regulators and Drivers** Tinto **Synthesisers and PLLs** Moorfoot **Impulse UWB Receivers** Kilsyth
10.50–11.20	Coffee break
11.20–12.40	**Low-Power Analogue** Tinto **Multi-Standard RF** Moorfoot **Short Range Low Data Rate Wireless Communications** Kilsyth
12.40–14.10	Lunch
14.10–14.50	**Joint plenary 6** V. Subramanian, Pentland
15.00–15.40	**ESSCIRC plenary 3** M. Berkhout, Pentland
15.40–16.10	Coffee break
16.10–17.50	**Sensor Interface Circuits** Tinto **High-Speed Digital Circuits and Systems** Moorfoot **RF Power Amplifiers and Radar** Kilsyth

General information

General organisation
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Deputy chair	Peter Ashburn, University of Southampton
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Deputy chair	Robert Henderson, University of Edinburgh
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Workshop chair	Anthony O'Neil, Newcastle University
ESS-fringe poster chairs	A J Snell, University of Edinburgh J T M Stevenson, University of Edinburgh
Local chair	Les Haworth, University of Edinburgh

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Rebecca Cheung	University of Edinburgh
Tom Stevenson	University of Edinburgh
Stewart Smith	University of Edinburgh
Jon Terry	University of Edinburgh

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Reinout Woltjer	(chair) NXP

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John Pennock	Wolfson

Ian Phillips	ARM
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Horst Zimmermann	TU Vienna

Welcome to Edinburgh

Edinburgh is located in the south-east of Scotland. It has been the capital of Scotland since 1437 and is the seat of the Scottish Parliament. Owing to its rugged setting and vast collection of medieval and Georgian architecture, including numerous stone tenements, it is often considered to be one of the most picturesque cities in Europe. The Old Town and New Town districts of Edinburgh were listed as a UNESCO World Heritage Site in 1995.

The city is well known for the annual Edinburgh Festival – a collection of official and independent festivals held annually over about four weeks starting in early August. Edinburgh is one of Europe's major tourist destinations, attracting around 13 million visitors a year, and it is the second most visited tourist destination in the UK, after London.

Climate

The climate in Edinburgh is relatively mild in September. However, the weather can change quickly throughout the day – a rainy morning can often be followed by a sunny afternoon. It is therefore advisable to come prepared for a mild but rainy climate.

Time zone

Western Europe daylight/summertime (GMT + 1:00)

Electricity

Requires UK standard three-pin plug, 220–240 V, 50 Hz.

Currency
The Scottish currency is the British Pound Sterling. Bank of England banknotes are accepted as legal currency, in addition to those issued by the Bank of Scotland, the Royal Bank of Scotland and the Clydesdale Bank. Some retail outlets and visitor attractions will also accept Euros.

Tips
It is customary to pay 10% in a restaurant or café, although this is only expected if there is waiter service. If it is a takeaway or self-service establishment you will not be expected to tip.

Banks
Most banks are usually open Monday to Friday from 09.30 to 16.00/17.00. Some larger branches may also be open later on Thursdays and on Saturday mornings. Avoid changing money or cheques in hotels because the rates are usually very poor.

Emergency calls
In case of emergency, dial 999 for the police or fire services.

Passport and visa
Visitors from some countries require a visa to enter the UK. Please check with your travel agent. Participants who require a visa should allow plenty of time for their application to be processed. The Institute of Physics can issue the standard letter of invitation to those participants with an accepted presentation at the conference and from whom payment has been received in full for their registration. For those not making a presentation, the Institute of Physics cannot issue invitation letters. Delegates will instead receive a letter confirming the conference details and confirmation of payment of registration.

Hotels

To arrange accommodation while at the conference, please contact BSI, quoting "IOP" (tel 0870 830 4266; e-mail IOP@bsi.co.uk). Information about all hotels can be found in the "Hotels" section of the websites at **www.essderc2008.org** and **www.esscirc2008.org**.

More information about the city is available on the Edinburgh Tourist Board website at **www.edinburgh.org**.

Conference site

The conference, tutorials, workshops and exhibition will be held at:

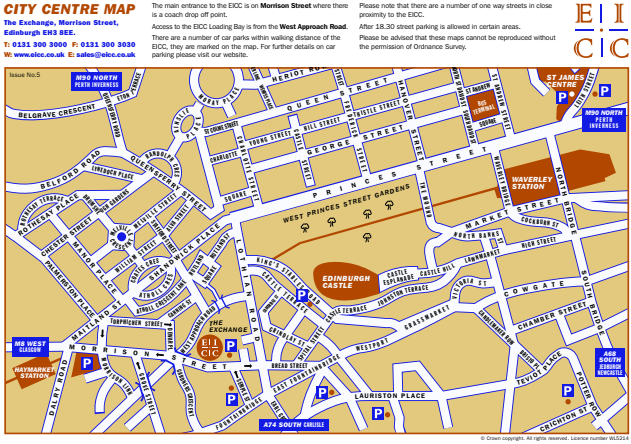
Edinburgh International Conference Centre (EICC)
The Exchange
Edinburgh EH3 8EE
Tel 0131 300 3000
www.eicc.co.uk
How to get to there
The Edinburgh International Conference is located at the heart of Scotland's capital city. Its prime central location ensures easy access via road, rail and air, and many of its famous and historical attractions are within walking distance. A range of hotels to suit all budgets and requirements are also within a short distance of the centre.

The EICC is arranged over four levels and part of its attraction is the versatility and space available. On arriving in the conference centre, you will find yourself in the Strathblane Hall, where you will be able to register for the conference.
By plane
For the latest information about flights to Edinburgh, visit the website at www.edinburghairport.com. There are a number of ways to travel into the city centre from the airport, as described below.
By taxi
There is an excellent taxi service direct from the airport to the city. You'll find official airport taxis at the taxi rank outside the terminal building (follow the signs inside the airport). It costs about £15 to get a taxi from the airport to the city centre and the journey takes around 20 minutes, depending on traffic flow and time of day.

Local taxi numbers
Computer Cabs
Tel 0131 272 8000
www.comcab-edinburgh.co.uk

Festival City Cars
Tel 0131 552 1777
www.festivalcitycars.co.uk

By coach
The Airlink 100 operates a frequent bus service (every 10 minutes at peak times) between Edinburgh Airport and the city centre, with



designated stops *en route*. Regular bus services start at 04.45 and run until 00.22 at night. The journey time is 20 minutes, with tickets costing £3.00 single and £5.00 return. Delegates are advised to disembark at Haymarket Railway Station and to follow signs for the EICC on foot (a five-minute walk). Also, the N22 bus departs from stand 19 and runs every 30 minutes through the night until the Airlink service starts again. For more information about these services, visit www.flybybus.com.

By Edinburgh Shuttle

The Edinburgh Shuttle is a door-to-door shared transport service between Edinburgh Airport and the city centre. Fares start at £8.00 for an individual with reduced rates for passengers travelling together to the same destination. Visit www.edinburghshuttle.com or tel 0845 500 5000.

Arriving by train

Edinburgh has two railway stations: Waverley and Haymarket. Waverley is the main station and has direct routes to many cities across the country. For more information, visit www.nationalrail.co.uk. Haymarket is just a five-minute walk from the EICC. Waverley is a few minutes away by taxi.

By bus

Edinburgh's main bus terminal is located at St Andrew's Square. Bus connections stretch right across the UK. For details of these routes, visit www.nationalexpress.com or www.citylink.co.uk.

By car

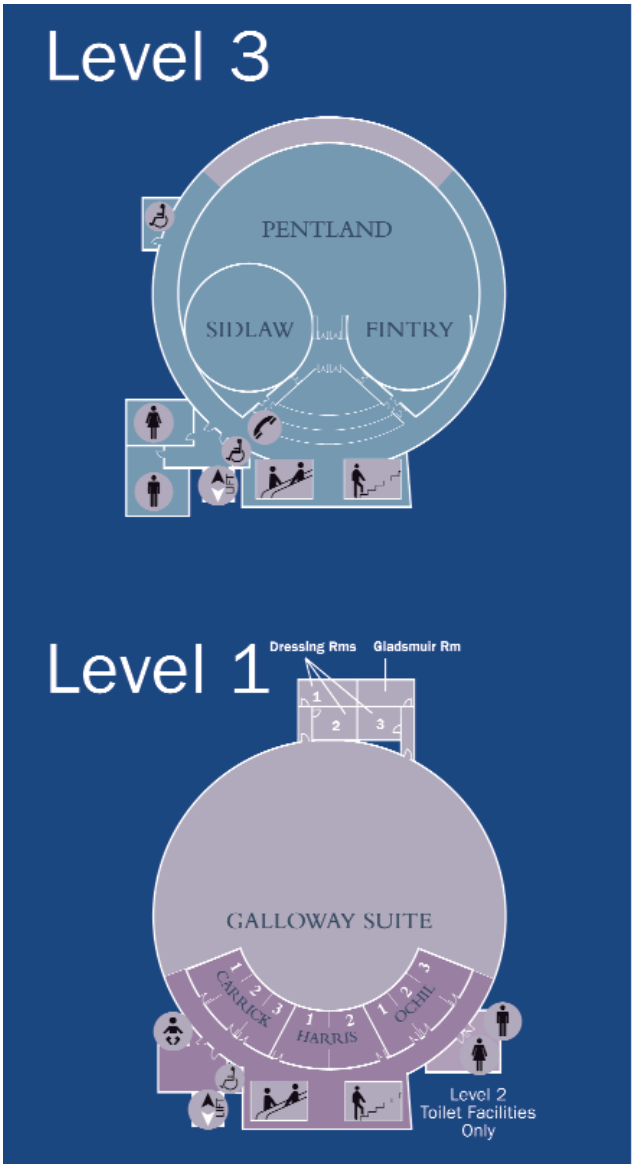
The EICC is right in the centre of Edinburgh. The main entrance is on Morrison Street. For directions from your home or office, visit

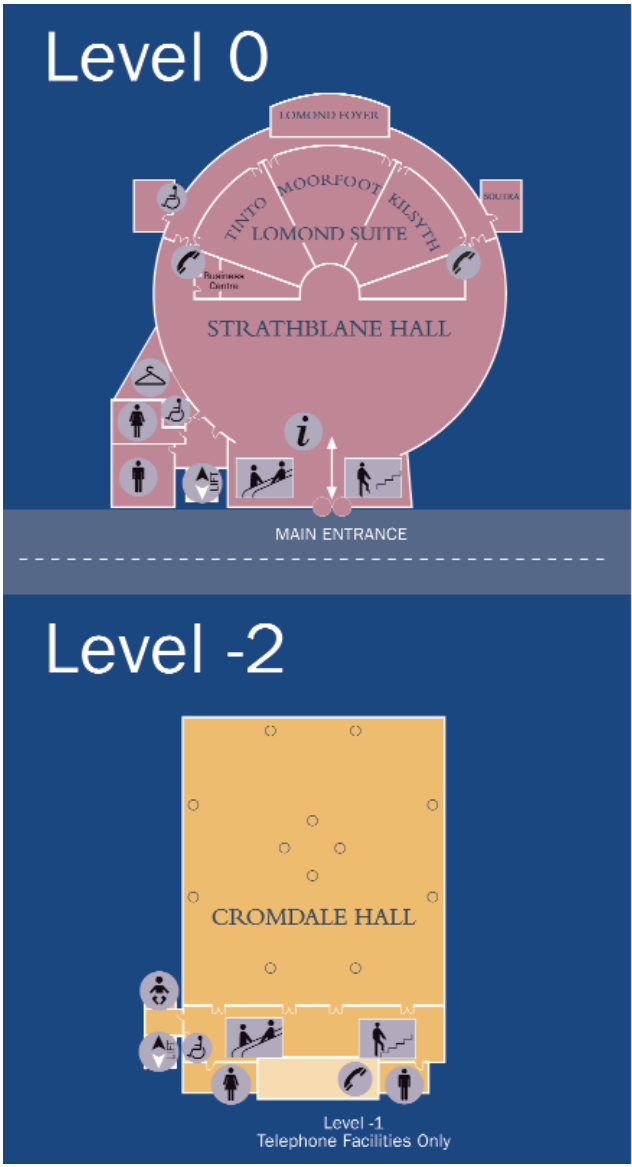
www.theaa.com and input EH3 8EE for the destination postcode into the route planner.

Local buses

Numbers 2 and 12 depart approximately 200 yards from the entrance to the EICC on Morrison Street and run every 15 minutes between 07.00 and 23.30. There are regular city bus services to Lothian Road and Shandwick Place. Delegates should follow directional signage from Lothian Road and Shandwick Place to the EICC. Buses require the exact change: £1.10 for any journey; day tickets are available for £2.30. For further information, visit the Lothian Buses website at **www.lothianbuses.co.uk**.

Conference venue




Level 0
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KILSYTH
LOMOND SUITE
SOUTRA
STRATHBLANE HALL
MAIN ENTRANCE
Level -2
CROMDALE HALL
Level -1
Telephone Facilities Only

Conference facilities

Car parks
There are a number of car parks, all within five minutes' walking distance from the EICC. Local car parks are highlighted on the EICC city centre map (p16).

Morrison Street car park
Capacity: 400 spaces.
Approximate rates: £1.00 (hourly rate)/£5.00 (4–6 h)/£7.20 (8 h)/£2.50 (from 17.00 until 07.00).
Contact: enquire at the registration desk or tel 0131 477 7000

Semple Street (Thistle Parking)
Capacity: 200 spaces.
Approximate rates: £1.00 (up to 6 h)/£8.00 (6–10 h)/£10.00 (more than 10 h)
Contact: tel 0131 225 7480

EICC Morrison Street
Capacity: 88 spaces
Approximate rates: £1.00 (up to 1 h)/£5.00 (4–6 h)/£7.20 (more than 8 h)/£2.50 (from 17.00 until 07.00)
Contact: enquire at the registration desk or tel 0131 477 7000

Castle Terrace
Capacity: 750 spaces
Open 24 hours
Approximate rates: £2.50 (up to 2 h)/£7.00 (4–6 h)/£10.50 (9–24 h)/£3.00 (from 17.00 until 06.00)
Contact: tel 0131 229 2870

Public phones
For outgoing calls, coin/card-operated phones are available in the Business and Media Centre on Level 0 and near the main escalator/stairs on Levels 2 and 3.

Cloakroom and toilets
Cloakroom facilities can be found next to the lifts in the Strathblane Hall on Level 0. Toilets can be found on every level of the conference centre next to the main escalators/stairs.

Left luggage
A left luggage area will be available at the cloakroom in the Strathblane Hall, particularly during peak times for delegate arrival

and departures. Please visit the registration desks near the cloakroom if you have any special requirements.

Drink and food facilities

There are coffee/tea machines throughout the venue, all of which accept cash. There is also an area in the Strathblane Hall selling soft drinks and light snacks.

Disabled access

Please contact the registration desk or make yourself known to a member of EICC staff, who will assist with any access or facility requirements.

Fire and evacuation procedures

Fire exits are located in each of the four corners of the building and are well signposted. In the unlikely event of an emergency, please leave the building in an orderly manner, as directed. Do not use the main stairs or escalators. On exiting the building, we will ask you to move to muster points as advised by the stewards and emergency marshals.

Conference registration

Conference registration desk
The registration desk will be situated in the Strathblane Hall and will be open throughout the conference at the following times:

Sunday	16.00–19.00
Monday	08.00–18.30
Tuesday	08.00–18.30
Wednesday	08.00–18.30
Thursday	08.00–18.30
Friday	08.00–18.00

On arrival, all participants will be given a registration pack containing conference material and a lapel badge, which must be worn at all times during the conference. Replacement badges can be issued at the registration desk.

To contact the ESSDERC-ESSCIRC registration desk, tel +44 (0)131 519 4123.

Messages
There will be a message board next to the registration desks in the Strathblane Hall. All messages must be given to a member of the conference team, who will then be able to post them on the board. Plasma screens throughout the EICC will broadcast up-to-date information about the technical programme.

Conference information

Internet access
Wireless internet access will be available throughout the EICC. This will be free of charge during the conference and exhibition, and passes can be collected from the registration desk throughout the event. For one-off access to a PC and the internet, there will be several computers in the Business and Media Centre, charged at an hourly rate.

Official language
The congress language is English.

Speakers briefing
Authors should meet their chairperson in the session room 20 minutes prior to the beginning of their respective sessions.

Conference proceedings
All participants will receive a copy of either the ESSDERC or the ESSCIRC Proceedings and a USB device containing the accepted papers for both.

Best Paper Award
ESSDERC/ESSCIRC offers a Best Paper Award (for contributed papers only) and a Young Scientist Award for the best paper presented by a speaker under the age of 28. Selection is based on evaluation by the audience and paper ratings.

Insurance disclaimer
Participants are responsible for their own insurance. The Institute of Physics, Trinity College and their approved representatives cannot take responsibility for any accident, loss or damage to participant or their property during the event.

Complaints
While we hope that your time at the conference is enjoyable, if you encounter a problem during your stay, please report it to the registration desk as soon as possible. The conference team will make every effort to rectify the issue.

Conference overview

Sunday 14 September 2008

Registration	Strathblane Hall

Monday 15 September 2008

Registration	Strathblane Hall
Tutorials	Harris 1, Moorfoot Suite, Kilsyth Suite, Tinto Suite
Buffet lunch	Strathblane Hall
Fringe	Cromdale Hall

Tuesday 16 September 2008

Registration	Strathblane Hall
Conference opening	Pentland Suite
Technical sessions	Pentland Suite, Sidlaw Suite, Fintry Suite, Carrick Suite, Harris 1, Ochil Suite, Tinto Suite, Moorfoot Suite, Kilsyth Suite
Buffet lunch	Cromdale Hall
Exhibition	Cromdale Hall
Fringe	Cromdale Hall
Welcome reception	Cromdale Hall
Women's event	University of Edinburgh

Wednesday 17 September 2008

Registration	Strathblane Hall
Technical sessions	Pentland Suite, Sidlaw Suite, Fintry Suite, Carrick Suite, Harris 1, Ochil Suite, Tinto Suite, Moorfoot Suite, Kilsyth Suite
Buffet lunch	Cromdale Hall
Exhibition	Cromdale Hall
Fringe	Cromdale Hall
Conference dinner	Murrayfield Stadium

Thursday 18 September 2008

Registration	Strathblane Hall
Technical sessions	Pentland Suite, Sidlaw Suite, Fintry Suite, Carrick Suite, Harris 1, Ochil Suite, Tinto Suite, Moorfoot Suite, Kilsyth Suite
Buffet lunch	Cromdale Hall
Exhibition	Cromdale Hall
Fringe	Cromdale Hall

Friday 19 September 2008

Registration	Strathblane Hall
Workshops	Sidlaw Suite, Carrick Suite, Harris 1, Harris 1, Ochill Suite, Tinto Suite, Moorfoot Suite, Kilsyth Suite
Buffet lunch	Stathblane Hall

Meals and refreshments

All meals and refreshments will be served at allocated times during the conference programme.

Monday 15 September 2008

Morning refreshments	Strathblane Hall
Buffet lunch	Strathblane Hall
Afternoon refreshments	Strathblane Hall

Tuesday 16 September 2008

Morning refreshments	Cromdale Hall
Buffet lunch	Cromdale Hall
Afternoon refreshments	Cromdale Hall
Welcome reception	Cromdale Hall

Wednesday 17 September 2008

Morning refreshments	Cromdale Hall
Buffet lunch	Cromdale Hall
Afternoon refreshments	Cromdale Hall
Conference dinner*	Murrayfield Stadium

Thursday 18 September 2008

Morning refreshments	Cromdale Hall
Buffet lunch	Cromdale Hall
Afternoon refreshments	Cromdale Hall

Friday 19 September 2008

Morning refreshments	Strathblane Hall
Buffet lunch	Strathblane Hall
Afternoon refreshments	Strathblane Hall

*The conference dinner is inclusive in the conference fee and must be prebooked. To reserve additional places, email faye.heran@iop.org in advance.

Social programme

Tuesday 16 September

Welcome reception

A welcome reception will take place from 18.30 to 20.30 in the Cromdale Hall. This will include a whisky-tasting session, offering delegates the opportunity to sample traditional whiskies and cheeses from across Scotland. Wine and soft drinks will also be available.

Tuesday 16 September

Women's event and dinner

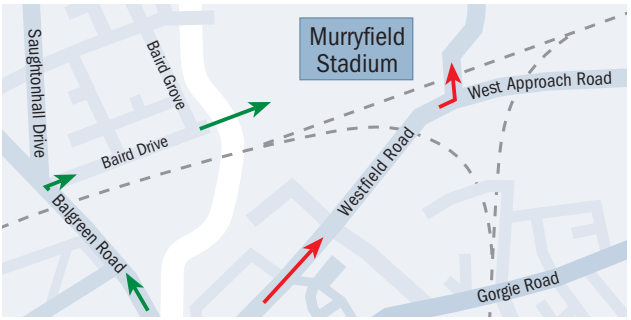
This will take place in the evening. For further details, please enquire at the registration desk during the conference or refer to the websites at www.essderc2008.org or www.esscirc2008.org.

Wednesday 17 September

Conference dinner

The conference dinner will be held at Murrayfield Stadium, the home of Scottish Rugby, from 19.00 to 01.00. It will consist of a three-course Scottish-themed menu in the Thistle and Presidential Suite and will be preceded by a Pitchside drinks reception (weather permitting) with traditional Scottish entertainment. Coaches will be provided to transport participants to and from the EICC.

Participants with special dietary requirements are asked to notify the conference organiser prior to their arrival. Unfortunately it will not be possible to provide an alternative menu unless prior notification has been received.
For further information about Murrayfield Stadium, visit the website at www.murrayfieldexperience.com



Travelling to the Murrayfield Stadium
Shuttle service
Coaches will be scheduled to take all delegates to and from Murrayfield Stadium at the following times:.

EICC to Murrayfield Stadium
There will be three pick-ups from the front of the EICC at 18.30, 19.00 and 19.30.

Murrayfield Stadium to EICC
A shuttle service will run between 22.30 and 24.00, picking up outside Murrayfield Stadium and dropping off outside the EICC and Princess Street. For all delegates returning after 24.00, it is advised that a private taxi is booked beforehand. Taxi numbers are provided on p15.

Independent travel
For those who wish to arrange independent travel to and from Murrayfield Stadium, details of the location and directions to the venue are provided below:

Murrayfield Experience
Edinburgh
Midlothian EH12 5PJ
Tel 0131 346 5250
E-mail enquiries@murrayfieldexperience.com

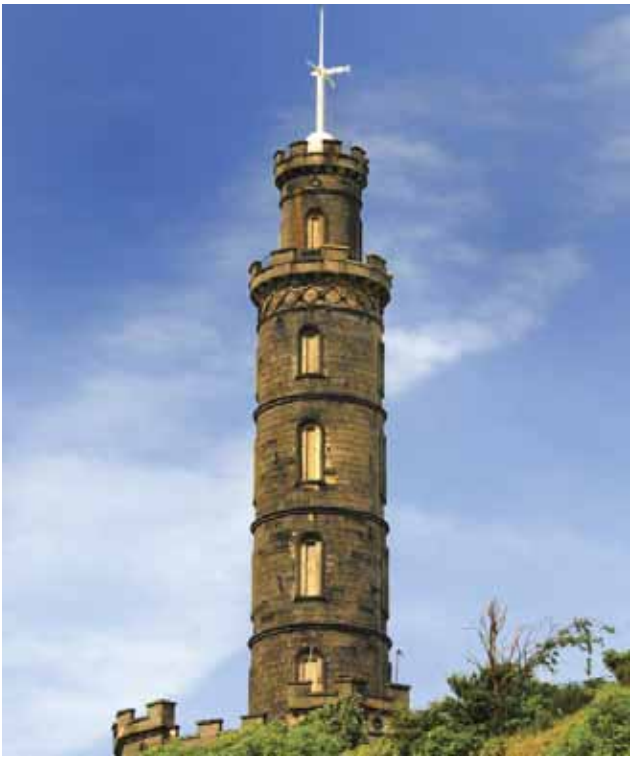
Murrayfield Stadium is situated in West Edinburgh, six miles from the International Airport, three miles from Edinburgh Waverley Railway Station, one mile from Haymarket Railway Station and close to the city bypass, and the M8 and M9 motorways.
A map of the location is provided below. Please note that the green arrows are for match-day routes and the red arrows are normal business days.

Accompanying persons programme

As a world-class tourist destination, the Edinburgh naturally offers a multitude of activities, whatever time of year you visit. Located within easy walking distance of the EICC, Edinburgh's Old Town is a fascinating district of cobbled streets, alleys and courtyards. The Royal Mile is a clear favourite with visitors, offering a variety of museums, shops and, of course, the world-famous Edinburgh Castle. Ghost tours take place every evening around the Old Town, alluding to perhaps the more sinister side of Edinburgh's past. Open-top bus tours are an excellent way of viewing the whole city. Linking the Old Town with the Royal Yacht Britannia, these explore Edinburgh's Georgian New Town and Holyrood Park. Simply hop on and off the bus to visit your favourite attractions.

A list of attractions can be found on the Edinburgh Tourist Board website at **www.edinburgh.org**. Some that we particularly recommend are listed below.

Dynamic Earth
Based in the heart of Edinburgh, Dynamic Earth tells the story of our planet's past, present and future.
Price per person: adult £9.50/child £5.95 (3–15 years)
Opening times: 10.00–18.00
www.dynamicearth.co.uk



Edinburgh Castle
The castle is the best known and most visited of historic buildings in the city. Perched on an extinct volcano and offering stunning views, this instantly recognisable fortress is a powerful national symbol and part of Edinburgh's world heritage site.
Price per person: adult £12.00/Child £6.00 (5–15 years)
Opening times: 09.30–18.00
www.edinburghcastle.gov.uk

Museum of Edinburgh
The Museum of Edinburgh, formerly known as Huntly House, occupies a series of picturesque 16th- and 17th-century buildings in the heart of the Old Town. It illustrates the history of the city from the earliest settlement to the present day.
Admission free
Opening times: 10.00–17.00 (Monday to Saturday)
www.cac.org.uk

National Museums Scotland
This family of attractions includes the National Museum of Scotland, the National War Museum, the National Museum of

Costume, the National Museum of Rural Life, the National Museum of Flight and the National Museums Collection Centre.
Price per person: varies from free admission to £8.50
Opening times: 10.00–17.00
www.nms.ac.uk

The Palace of Holyroodhouse
Founded as a monastery in 1128, the palace is The Queen's official residence in Scotland. Situated at the end of the Royal Mile, the it is closely associated with Scotland's turbulent past, including Mary, Queen of Scots, who lived here between 1561 and 1567. Successive kings and queens have made the Palace of Holyroodhouse the premier royal residence in Scotland.
Price per person: adult £9.80/child £5.80 (5–17 years)/free (under 5 years)
Opening times: 09.30–18.00 (last admission 17:00)
www.royal.gov.uk

Edinburgh Zoo
The largest and most exciting wildlife attraction in Scotland, the zoo is committed to the highest standards of animal welfare, conservation and environmental education.
Price per person: adult £11.50/child £8.00 (3–14 years)/free (under 3 years)
Opening times: 09.00–18.00
www.edinburghzoo.org.uk

Time Out guide
Time Out provides an up-to-date guide to accommodation and attractions, a current events calender and restaurant reviews. The guide for Edinburgh can be found online at **www.timeout.com/travel/edinburgh.**

Edinburgh pass
The Edinburgh pass offers free travel, plus discounts on shopping, meals and visitor attractions around the city, together with a comprehensive guidebook. Passes range from one to three days and can be purchased online at **www.edinburgh.org/pass**, which also offers maps, information about the city and suggested itineries for a short visit.

Exhibition

Hosted by JEMI UK
www.jemiuk.com

The exhibition is a new addition to the ESSSDERC/ESSCIRC format and will include representation from a number of equipment and materials suppliers as well as major scientific publishers. It will take place in the Cromdale Hall on Level 2 and will run from Tuesday 16 To Thursday 18 September. All refreshment and lunch breaks will be hosted in the exhibition area during the main conference days, together with the welcome reception on Tuesday 16 September and the fringe sessions.

A separate exhibition handbook will be produced and can be collected from the registration desk on arrival.

Opening hours

Tuesday 16 September	08:00–18:00
Wednesday 17 September	08:00–18:00
Thursday 18 September	08:00–18:00

Exhibition organisers

Ingrid Prince
Business manager
JEMI UK Ltd
Tel +44 (0)131 650 7815
Fax +44 (0)131 650 7475
E-mail jemi-enquiries@see.ed.ac.uk

Joint plenary talks

Emerging Device Nanotechnology for Future High-Speed and Energy-Efficient VLSI: Challenges and Opportunities
Chau, Robert
Intel Corporation

Technology Interfacing for Fabless Semiconductor Companies
Manian, Vahid
Broadcom

Micropower Energy Scavenging
van Hoof, Chris
IMEC

Solving Issues of Integrated Circuits by 3D-Stacking Meeting with the Era of Power, Integrity Attackers and NRE Explosion and a Bit of Future
Sakurai, Takayasu
University of Tokyo

More Than Moore and More Moore in Europe
Michael Thompson
STMicroelectronics

Printed Electronics for Low-Cost Electronic Systems: Technology Status and Application Development
Subramanian, Vivek
University of California, Berkeley

For a complete abstract description of the joint plenary talks (p00), plus locations and times (p00), see the ESSDERC programme.

ESSCIRC plenary talks

Information, Energy, and Entropy: Design Principles for Adaptive, Therapeutic Modulation of Neural Circuits
Denison, Timothy
Medtronic

This paper discusses the challenges and opportunities designing technology for deep brain stimulation (DBS). DBS is currently approved for the treatment of movement disorders such as Parkinson Disease, essential tremor and dystonia, and a number of studies are underway to determine its clinical efficacy for the treatment of epilepsy, treatment resistant depression, and obsessive compulsive disorder (OCD).

Timothy Denison based in Minneapolis, Minnesota, Medtronic Inc. is the world's largest medical technology company. Founded in 1949, and credited with inventing the first wearable artificial pacemaker, the company now makes a wide array of implantable electronic devices, from cardioverter-defibrillators, to devices for managing urinary incontinence and obesity. They employ 37 000 people worldwide.

SOI Design in Cell Processor and Beyond
Hagihara, Yoshiaki
AIPS/AINS Consortium

A brief historical overview of the microelectronics of the present home entertainment LSI chips with regard to the product specifications and performance aspects of the home entertainment LSI chip sets, such as for digital cameras, home robotics and games are given in order to explore the possible killer applications as our driving force for our future semiconductor and electrical and electronic industries.

Yoshiaki Hagihara received his BS, MS and PhD in 1971, 1972 and 1975 respectively from California Institute of Technology Pasadena, California. His life-long interest is artificial intelligent systems including Robotic Visions and Operations. He joined Sony Tokyo Japan on February 1975 serving as a pioneering engineer for the CCD image sensor developments and its video camera systems. In 1980s till late 1990s he served as an engineering manager and later as the general manager for embedded SRAM, DRAM and NVRAM designs for MCU and application specific system LSI chips. Since 1995, he served as a Semiconductor R/D strategic planning Executive Staff, later as Sony Fellow and the general magager and the Head of Sony's Semiconductor Strategic Planning, responsible and also serving as technical advisors to Sony's Semiconductor domestic and global R/D and business and R/D developments, including the recent Sony-Toshiba-IBM project. He also served as Program Chair, Operational and Executive Committee member of many international IEEE conference including ICMTS, CoolChips Workshop, Vail Computer Element Workshop and also ISSCC. He retired Sony Tokyo Japan at the end of July 2008. He is now serving as the CEO and the President of the AIPS (Artificial Intelligent Partner Systems) Consortium, Atsugi-city Japan. He is an IEEE fellow.

Audio at Low and High Power
Berkhout, Marco
NXP Semiconductors

An overview is presented of recent developments in the analog boundaries of the audio chain. The main focus is on class-D amplifiers that are by now almost standard in consumer applications and emerging in automotive and mobile applications as well. Further, an overview of the state-of-the-art in A/D and D/A conversion is given.

Marco Berhout was born in Harderwijk, The Netherlands, in 1968. He received the M.Sc. degree in electrical engineering in 1992 and the Ph.D. degree in 1996, both from the University of Twente, Enschede, The Netherlands. Subsequently, he joined Philips Semiconductors, (now NXP Semiconductors) in Nijmegen where he is currently working as a Senior Design Engineer in the Analog Audio group. His main interests include class-D amplifiers and integrated power electronics.
NXP Semiconductors was formed in 2006 from the Semiconductor Division of Royal Philips Electronics N.V., and manufactures semiconductors and systems for markets including automotive, personal communication, identification and home electronics. It has approximately 37 000 employees.

ESSCIRC tutorials

Tutorial 4: Filter Design
AM Kilsyth Room
Organiser: Peter Mole

The tutorial is aimed at engineers early in their careers who have a need to design integrated filters either as a part of a university research project, or as a design project within industry. The course will assume a first degree level working knowledge of electronic engineering. It will refresh basic filter theory, and then progress to give practical implementations of both analogue and digital filters.

Agenda

08.30–09.45 **Filter Theory** Bram Nauta, University of Twente, Netherlands

10.00–10.45 **Tuning and Reconfiguration for Analog Filters** Andreia Cathelin, ST Microelectronics, Crolles, France

11.00–12.15 **Discrete Time Including Digital Filters** Markus Helfenstein, NXP, Zurich, Switzerland

12.15–12.30 **Question-and-answer session**

Filter Theory
Speaker: Bram Nauta, professor of Electrical Engineering at the University of Twente, Netherlands

Topics:
Amplitude and group delay responses:
● Comparison of standard filter forms: Butterworth, Bessel, Elliptic, Tchebychev, etc.
Filter synthesis – from mathematical formula to circuit representation:
● signal flow graph theory;
● sensitivity to design parameter;
● state space synthesis.
Non-idealities in filters (noise, distortion, phase error); improvements through filter topology choice
● noise;
● distortion;
● phase errors.
Practical comments on implementation of building blocks.

Tuning and Reconfiguration for Analog Filters
Speaker: Andreia Cathelin, ST Microelectronics, Crolles, France

Topics:
Influence of process, voltage and temperature variations on filter behavior
Tuning/trimming methodology: direct, indirect methods
● Implementation theory: on the use of the Master-Slave technique (PLL, ALL, etc...)
– Basic principles
– Possible limitations

– Alternative solutions

● Physical implementation examples on Gm-C filter circuits for mobile communications applications in zero-IF architecture

System need for reconfigurable filter architectures
Reconfigurable filter concept: work methodology
● Physical implementation examples on Gm-C filter circuits for mobile communications applications in zero-IF architectures

Discrete Time Including Digital Filters
Speaker: Markus Helfenstein, NXP, Zurich, Switzerland

Topics:
An introduction to discrete time signals
● Basic z- transform properties
● Time to frequency domain transformation
● The need for anti-aliasing/ reconstruction filters.
Discrete time, Analog filters - a brief overview of switched-cap filters
Design techniques for digital filters
● DFT/FFT filter structures
● Windowing techniques
● Linear phase design
● FIR/IIR design

Examples:
Two examples will be “walked through” to illustrate the above techniques:
● FIR filter eg 2.5G RX filters
● Audio codec digital filtering -digital biquad

Question-and-answer session
A period of 15 minutes will be allocated at the end of the tutorial when questions can be asked of the lecturers.

Biographies
Bram Nauta received the M.Sc degree (cum laude) in electrical engineering from the University of Twente, Enschede, The Netherlands, and his Ph.D. degree from the same university on the subject of analog CMOS filters for very high frequencies. In 1991 he joined Philips Research, where he worked on high speed AD converters and analog key modules. In 1998 he returned to the University of Twente, as full professor heading the IC Design group. His current research interest is high-speed analog CMOS circuits. He is Editor-in-Chief for the IEEE Journal of Solid-State Circuits. He is also member of the technical program committees of the International Solid State Circuits Conference (ISSCC), the European Solid State Circuit Conference (ESSCIRC), and the Symposium on VLSI circuits. He is co-recipient of the ISSCC 2002 "Van Vessem Outstanding Paper Award", is distinguished lecturer of the IEEE, elected member of IEEE-SSCS AdCom and is IEEE fellow.

Andreia Cathelin started her electronic studies at the Polytechnic Institute of Bucarest, Romania and graduated from the Institut Supérieur d’Electronique du Nord (ISEN), Lille, France in 1994. From 1994 till 1998, she prepared a Ph. D. thesis with IEMN/ISEN, Lille, France and MS2 Company, Roubaix, France on a fully-integrated BiCMOS low power – low voltage FM/RDS receiver. From 1997 till 1998, she was with Info Technologies, Gradignan, France, working on analog and RF communications design. Since 1998, she is with ST Microelectronics, Crolles, France, now in the Technology R&D, Central CAD and Design Solutions,

CMOS System Architecture RF design team in Minatec, Grenoble. She is a senior design expert and her major fields of interest are RF and mmW systems for wireless communications, MEMS devices co-integration and SOI technologies.

Markus Helfenstein received the Bachelor degree from the Inst. of Technology in Lucerne in 1986, the diploma and the Dr. Sc. Techn. degree in electrical engineering from the Swiss Federal Institute of Technology in 1992 and 1997. In 2007 he also earned an executive MBA from the University of Fribourg, Switzerland.
From 1986 to 1988 he was with Mettler Instrumente AG, Switzerland, involved in the design of high resolution counter IC chips. Between 1996 and 1998 he was a lecturer for digital signal processing at the Inst. of Technology in Lucerne. In 1998, he co-founded Anadec GmbH, a start-up company which holds patents on the design of analog VLSI iterative decoders. Between 2000 and 2002 he was with Globespan Inc. (now Conexant) involved in projects on the design of mixed-signal chips for xDSL applications. He joined the Cellular Systems team of Philips (now NXP) in 2002. He is now a development manager at NXP and involved in projects utilising GSM/EDGE/UMTS mixedsignal
chips. He is a past associate editor of the Transactions on Circuits and Systems (TCAS-II) and he is member of the technical program committee of the European Solid State Circuit Conference (ESSCIRC).

Tutorial 5: PLL Design
PM Kilsyth Room
Organiser Peter Mole

The tutorial is aimed at engineers early in their careers who have a need to design a phase locked loop either as a part of a university research project, or as a design project within industry. The course will assume a first degree level working knowledge of electronic engineering. It will introduce the phase locked loop and the general theory of the loop, and then progress to give practical implementations of all the components of the loop for a variety of different applications.

Agenda

13.30–15.00 **The PII Loop** Carlo Samori, Politecnico di Milano, Italy

15.30–16.00 **Example 1: The Radio Synthesiser** Carlo Samori, Politecnico di Milano, Italy

16.00–16.30 **Example 2: Clock Recovery from a Pseudo Random Bit Stream** Ivan Bietti, ST Microelectronics, Crolles, France

16.30–17.00 **Example 3: Digitial PII for Clock Generation** Jan-Peter Frambach, NXP Nijmegen, Netherlands

17.00–17.15 **Question-and-answer session**

The PII Loop
Speaker: Carlo Samori, Politecnico di Milano, Italy

Topics:
- The PLL loop as a phase feedback system
- Analysis of the loop. Type I and type II definition
- Charge pump PLL

- Phase/frequency detection
- Discrete time effects the Gardner's limit to bandwidth
- Noise in the loop – relationship between noise and Jitter.
- Spurs in PLL
- Components of the loop, how their performance influences the overall loop

Phase/frequency comparison
– The VCO – sensitivity, phase noise
– The loop filter
– The fixed divider

Example 1: The Radio Synthesiser
Speaker: Carlo Samori, Politecnico di Milano, Italy

Topics:
- Offset PLL
- The fractional n- divider, fractional spurs
- Sigma delta control of the division ratio
- Examples of practical realisations

Example 2: Clock Recovery from a Pseudo Random Bit Stream
Speaker: Ivan Bietti, ST Microelectronics

- Jitter in Pseudo random bit streams, Jitter tolerance
- Detecting phase – the Hogge detector and bang bang detector

Example 3: Digital PLL for Clock Generation
Speaker: Jan-Peter Frambach, NXP Nijmegen, The Netherlands

Topics:
- Analog vs Digital PLL; the essential differences
- s an Analog PLL really a PLL?
- DPLL; a true phase domain loop
- Types of DPLL's
- True phase domain PLL
- Bang-bang PLL
- DPLL building blocks
- Time-to-Digital converter
- Phase detector
- Narrow Band / Wide Band DPLL

Biographies
Carlo Samori Received the PhD in Electrical Engineer and Communication from the Politecnico di Milano, where he is now an Associate Professor. His main research interests are in the field of low-phase noise VCO and PLL architectures.

Ivan Bietti received the degree in electronic engineering from the University of Pavia, Pavia, Italy in 1992. In the same year he joined SGS-Thomson Microelectronics in Agrate, Milan, Italy, where he was involved in the design of analog and mixed analog/digital integrated circuits for telecommunications. From 1996 to 1998 he was in Dublin, Ireland, working for the same company in the Computer and Peripherals Group designing analog CMOS filters, equalizers and PLLs for Disk Drives read/write channels. In 1999 he joined the RF group within the "Studio di Microelettronica" in Pavia where he led a research group working on the design of high speed Frequency Synthesizers and Low Noise Amplifiers mainly for mobile telecom applications. Since 2005 he moved to Grenoble, France, where he is currently responsible of the High Speed Serial

Interfaces design for the STMicroelectronics Data Storage Division. Recently hi is also taking care of the development of the analog part of the Read/Write Channel for Hard Disk Drive applications.

Jan Peter Frambach received the M.Sc. degree from Delft University of Technology (TUD), The Netherlands, in 1994. He joined Philips Semiconductors in 1995. He has worked on Optical Networking BiCMOS chipsets up to 10Gbit/s; Wideband Amplifiers, Data & Clock Recovery, High Speed (De)Serializers, Cross Point Switches. Since 2003 he has been developing wireless integrated transceivers in RF-CMOS. His current research interests are: Oscillators (RF and LF), PLL's, Data Converters and PA's. Currently he is leading the Bluetooth 45nm Transceiver development team at NXP Semiconductors.

Tutorial 6: All you want to know about RF CMOS - 1 GHz to 0.1THz
All day Tinto Room
Organiser: Peter Mole

The short course is aimed at making practising engineers aware of the rapid advances that are occurring in RFCMOS as the line widths reduce below 90nm. This has pushed the upper frequency capability towards 0.1THz. With this move up in frequency, there is a necessity to refine measurement techniques to get signals on and off the chip, to improve modelling of device behaviour, improve modelling of passive structures to guide the signal on the chip and to select architectures that lend themselves to CMOS implementation. In this course experts will present these skills which are essential for design new frequency limits and will improve understanding at lower frequencies

Agenda

09.00–09.50 **Making Measurements on Chip at 50–100 GHz** Mikko Kantanen, MilliLab, Finland

09.50–10.40 **Construction, Modelling and Characterisation of Passives on Silicon for RF and Millimetre Wave Applications** John R. Long, Electronics Research Laboratory/DIMES, Delft University of Technology, Netherlands

11.00–11.50 **RF Modelling of MOS Transistors for 0.1 THz Operation** Christian Enz, EPFL, Switzerland

11.50–12.20 **RF Circuits for UWB, 3 GHz to 10 GHz** Domine Leenaerts, NXP, Eindhoven

12.20–13.30 Lunch

13.30–14.00 **Design of Amplifiers and Mixers in Baseline CMOS Technology** Mikko Varonen, Helsinki University of Technology

14.00–14.30 **Millimeter Wave Design in Bulk and SOI CMOS** Andreia Cathelin, ST Microelectronics, Crolles, France

14.30–15.20 **RF Assembly and Packaging – Ongoing System Integration** Klaus Pressel, Infineon Technologies, Regensburg, Germany

15.45–16.35 **RF Radio Architectures/System Design for CMOS Applications** Hooman Darabi, Broadcom Irvine California, USA

16.35–16.50 **Question-and-answer session**

Making Measurements on Chip at 50–100 GHz
Speaker: Mikko Kantanen, MilliLab, Finland

Topics:
● On-wafer s-parameter, linearity, noise figure, and noise parameter measurement techniques up to 110 GHz.
● On-wafer interface: signal routing using waveguides or thin coax cables, requirements to circuit design to make measurements easier.
● Most common on-wafer calibration techniques for millimetre wave s-parameter measurements.
● Typical measurement set-ups with practical considerations are described using examples.

Construction, Modelling and Characterisation of Passives on Silicon for RF and Millimetre-Wave Applications
Speaker: John R. Long, Electronics Research Laboratory/DIMES, Delft University of Technology, Netherlands

Topics:
● Modelling, simulation, physical layout and design of monolithic passive elements for RF and high-speed applications.
● Circuit models for RLC components, interconnect wiring (including microstrip and coplanar waveguide) and other distributed parameter passive elements, such as transformers and transformer baluns.
● Simulation of passive components with traditional IC simulation tools, such as SPICE and other RF simulators (e.g. Agilent-ADS).
● The limitations and advantages of on-chip passives to the circuit designer at microwave and millimetre-wave frequencies are described using case-studies from transceiver applications.

RF Modelling of MOS Transistors for 0.1 THz Operation
Speaker: Christian Enz, Professor Electronic Engineering, EPFL, Switzerland

Topics:
● Compact modeling status
– From threshold-based models to charge and surface potential models (PSP, BSIM4, EKV)
● Static charge-based model
– Basic long-channel model
– Physical effects important at 90 nm and below (DIBL, gate current, mobility reduction, velocity saturation)
● What changes at RF?
– Limit from quasi-static to non-quasistatic operation
– Common figures of merit (ft, fmax, Fmin)
● Small-signal charge-based model
– Intrinsic and extrinsic parts
– Gate resistance
– Substrate network
● Noise model
– Channel thermal noise
– Induced gate noise
– Gate current noise
– Flicker noise

– Noisy two-port parameters

RF Circuits for UWB, 3GHz to 10GHz
Speaker: Domine Leenaerts NXP, Eindhoven

Topics:
● Presentation of designs of LNA, frequency divider and full receiver chain for UWB.
● Comparison of circuit performance over process nodes (90 nm, 65 nm and 45 nm).
● Comparison of RF measures (ft, ftmax, NFmin) over the same process nodes Including real effects of device connections.

Design of Amplifiers and Mixers in Baseline CMOS Technology
Speaker: Mikko Varonen Helsinki University of Technology

Topics:
● The design flow and methodology of millimeter-wave integrated circuits in baseline CMOS technology are discussed.
● The simulation and measurement results of active and passive test structures such as transistors, coplanar waveguides, capacitors and a spiral transmission line balun are presented.
● The design of millimeter-wave CMOS amplifiers are discussed.
● The design of millimeter-wave up and down conversion mixer circuits are discussed.
● Measurement results of implemented CMOS amplifiers and mixers are presented.

Millimeter Wave Design in Bulk and SOI CMOS
Speaker: Andreia Cathelin, ST Microelectronics, Crolles, France

Topics:
● Target applications for the Millimeter-wave frequency band
● Silicon technologies to address mmW complete solutions
● Active devices on bulk and SOI technologies
● LNA mmW designs Down-conversion mixers for mmW
● Voltage controlled oscillators for mmW
● Power amplifiers for mmW
● Conclusions

RF Assembly and Packaging – Ongoing System Integration
Speaker: Klaus Pressel, Infineon Technologies, Regensburg, Germany

Topics:
● Overview on basic package technologies including: flip chip and wire bonding and their RF capabilities is given.
● Technologies considered include thinning, dicing, shielding, heat dissipation, and stacking into the third dimension. The impact of warpage, especially for system-in-package, is considered.
● An innovative assembly and interconnect solution based on wafer level packaging allowing improved RF performance – also for ≤ 65 nm technologies – both for SoC and SiP is presented.
● Choices to integrate passive components are discussed.
● The impact to consider also the package/board interface is taken into account.
● We show examples for CMOS devices and for SiGe based devices with frequencies up to the mm-wave range (about 80 GHz).

● The importance of coherent chip/package/board co-design is highlighted. All these developments require the involvement of chip and assembly and package design teams from the very beginning of product design

RF Radio Architectures/System Design for CMOS Applications
Speaker: Hooman Darabi, Broadcom Irvine California

Topics:
● General system level concerns for CMOS transceivers are described. For example, linearity, frequency planning, blockers and spurious mixing.
● Various radio architectures suitable for different standards, such as cellular, Bluetooth and WLAN are presented, and the trade-offs are discussed.
● Question-and-answer session – a period of 15 minutes will be allocated at the end of the tutorial when questions can be asked of the lecturers.

Biographies
Mikko Kantanen received his Master of Science (Tech.) and Licentiate of Science (Tech.) degrees in Electrical Engineering from Helsinki University of Technology (TKK), Espoo, Finland 2001 and 2006, respectively. He is currently working towards the Ph.D. degree. Since 2001 he has worked as a Research Scientist in MilliLab, VTT Technical Research Centre of Finland, Espoo, Finland, in the areas of millimeter wave integrated circuit design, millimeter wave measurements, and millimeter wave systems. Mr. Kantanen is a recipient of an Asia-Pacific Microwave Conference 2006 Prize.

John Long received the M.Eng. and Ph.D. degrees in Electronics from Carleton University in 1992 and 1996, respectively. He worked for 12 years at Bell-Northern Research on Gbit/s fiber systems, and for 5 years at the University of Toronto. In 2002, he joined the Delft University of Technology as Chair of the Electronics Research Laboratory. His current research interests include: mm-wave IC design, low-power transceiver circuitry for broadband and highly-integrated radios, and electronics for high-speed datacomm systems.

Christian Enz (M'84) received the M.S. and Ph.D. degrees in electrical engineering from the Swiss Federal Institute of Technology, Lausanne (EPFL) in 1984 and 1989 respectively. From 1984 to 1989 he was research assistant at the EPFL, working in the field of micropower analog CMOS integrated circuits (IC) design. In 1989 he was one of the founders of Smart Silicon Systems S.A. (S3), where he developed several low-noise and low-power ICs, mainly for high energy physics applications. From 1992 to 1997, he was an Assistant Professor at EPFL, working in the field of low-power analog CMOS and BiCMOS IC design and device modeling. From 1997 to 1999, he was Principal Senior Engineer at Conexant (formerly Rockwell Semiconductor Systems), Newport Beach, CA, where he was responsible for the modeling and characterisation of MOS transistors for the design of RF CMOS circuits. In 1999, he joined the Swiss Center for Electronics and Microtechnology (CSEM) where he launched and lead the RF and Analog IC design group. In 2000, he was promoted Vice President, heading the Microelectronics Department. He is also lecturing and supervising undergraduate and graduate students in the field of analog and RF IC design at EPFL, where he is Professor since 1999. His technical interests and expertise are in the field of very low-power analog and RF IC design and semiconductor device modeling, with a particular focus on noise. He is the author and co-author of more than 140 scientific papers and has contributed to numerous conference presentations and advanced engineering courses. Together with E. Vittoz and F. Krummenacher he is one of the developer of the EKV MOS transistor model and the author of the book "Charge-Based MOS Transistor Modeling - The EKV Model for Low-Power and RF IC Design" (Wiley, 2006). He is

member of several technical program committees, including International Solid-State Circuits Conference (ISSCC) and European Solid-State Circuits Conference (ESSCIRC). He has served as a vice-chair for the 2000 International Symposium on Low Power Electronics and Design (ISLPED), exhibit chair for the 2000 International Symposium on Circuits and Systems (ISCAS) and is chair of the technical program committee for the 2006 European Solid-State Circuits Conference (ESSCIRC). He is a member of IEEE and Chair of the IEEE Solid-State Chapter of West Switzerland.

Domine M. W. Leenaerts (M'94-SM'96-F'2005) received the Ph.D. degree in electrical engineering from Eindhoven University of Technology, Eindhoven, the Netherlands, in 1992.
From 1992 to 1999, he was with Eindhoven University of Technology as an Associate Professor with the Micro-electronic Circuit Design group. In 1995, he was a Visiting Scholar with the Department of Electrical Engineering and Computer Science, University of California, Berkeley. In 1997, he was an Invited Professor with the Technical University of Lausanne (EPFL), Lausanne, Switzerland. From 1999 until 2006, he has been with Philips Research Laboratories. Since 2007 he is with NXP Semiconductors, Research as senior principal scientist, involved in RF integrated transceiver design. He has published over 150 papers in scientific and technical journals and conference proceedings and holds over 20 US patents. He has coauthored several books, including Circuit Design for RF Transceivers (Boston, MA: Kluwer, 2001). Dr. Leenaerts served as IEEE Distinguished Lecturer in 2001-2003 and served as Associate Editor of the IEEE Transactions on Circuits and Systems-Part I (2002-2004). Since 2005 he is the IEEE Circuits and Systems Society Member representative in the IEEE Solid-State Circuits Society Administrative Committee. Since 2007 he serves as Associate Editor of the IEEE Journal of Solid-State Circuits. He is member of the technical program committees of ISSCC, ESSCIRC, and RFIC.

Mikko Varonen received the M.Sc. and Lic.Sc. degrees in electrical engineering from the Helsinki University of Technology (TKK), Espoo, Finland, in 2002 and 2005, respectively. He is currently working toward the Ph.D. degree in electrical engineering at the Electronic Circuit Design Laboratory, Helsinki University of Technology. His research interests involve millimetre-wave integrated circuits. He was the co-recipient of the APMC 2006 Prize for the outstanding contribution to the Asia-Pacific Microwave Conference.

Andreia Cathelin started her electronic studies at the Polytechnic Institute of Bucarest, Romania and graduated from the Institut Supérieur d'Electronique du Nord (ISEN), Lille, France in 1994. From 1994 till 1998, she prepared a Ph. D. thesis with IEMN/ISEN, Lille, France and MS2 Company, Roubaix, France on a fully-integrated BiCMOS low power – low voltage FM/RDS receiver. From 1997 till 1998, she was with Info Technologies, Gradignan, France, working on analog and RF communications design. Since 1998, she is with ST Microelectronics, Crolles, France, now in the Technology R&D, Central CAD and Design Solutions, CMOS System Architecture RF design team in Minatec, Grenoble. She is a senior design expert and her major fields of interest are RF and mmW systems for wireless communications, MEMS devices co-integration and SOI technologies.

Klaus Pressel received his PhD from the University of Stuttgart on investigations of point defects in III/V semiconductor devices. He worked for 8 years at the IHP Frankfurt (Oder) on both Si CMOS and SiGe:C research and technology. He was a department head for „Material, Diagnostics, Foundry", and strongly supported the set-up of analogue and digital circuit design capability. With his team Klaus

was responsible for characterisation of IHP's SiGe:C BiCMOS technology, reliability, testing, SPICE parameter extraction etc. In 2001 Klaus joined Infineon Technologies, where he focuses now on innovations in assembly and interconnect technology. His special interests are System-in-Package solutions and high frequency applications. Klaus is representing Infineon in the European MEDEA+/CATRENE steering group technology, EURIPIDES technical committee, ITRS, and JISSO. He has a long term experience in European and German funded research projects to look into future technologies. He is author/co-author of more than 100 papers/publications in semiconductor physics and technology, circuit design, assembly and interconnect technologies.

Hooman Darabi received the Ph.D. degree in electrical engineering from the University of California, Los Angeles in 1999. He is currently a director, engineering, with Broadcom Corporation, Irvine, CA. His interests include analog and RF IC design for wireless communications, including Bluetooth, WLAN, and cellular applications.

ESSCIRC programme

Tuesday September 16

08.50 **Introduction to ESSDERC & ESSCIRC 2008**

A1L-A **JOINT PLENARY – R. Chau**
Pentland
Chair(s): Anthony Walton, University of Edinburgh
Stephen Hall, University of Liverpool

A1L-A1 **Emerging Device Nanotechnology for Future High-Speed and**
09.00 **Energy-Efficient VLSI: Challenges and Opportunities**
Robert Chau, Intel Corporation, USA

A2L-A **Process Variablilty and Yield – Joint Session**
Pentland
Chair(s): Asen Asenov, University of Glasgow

A2L-A1 **Experimental Assessment of Logic Circuit Performance**
09.50 **Variability with Regular Fabrics at 90nm Technology Node**
Author(s): Sungdae Choi, University of Tokyo; Katsuyuki Ikeuchi, University of Tokyo; Hyunkyung Kim, University of Tokyo; Kenichi Inagaki, University of Tokyo; Masami Murakata, Semiconductor Technology Academic Research Center; Nobuyuki Nishiguchi, Semiconductor Technology Academic Research Center; Makoto Takamiya, University of Tokyo; Takayasu Sakurai, University of Tokyo

A2L-A2 **Area/Yield Trade-Offs in Scaled CMOS SRAM Cell**
10.10
Author(s): Vasudha Gupta, Mohab Anis, University of Waterloo

A2L-A3 **Evaluation of Intrinsic Parameter Fluctuations on 45, 32 and**
10.30 **22nm Technology Node LP N-MOSFETs**
Author(s): Binjie Cheng, Scott Roy, Andrew Brown, Campbell Millar, Asen Asenov, University of Glasgow

A2L-D **Power Converters**
Tinto
Chair(s): Erik Bruun, Technical University of Denmark

A2L-D1 **A Monolithic Step-Down SC Power Converter with Frequency-**
09.50 **Programmable Subthreshold Z-Domain DPWM Control for Ultra-Low Power Microsystems**
Author(s): Ling Su, Dongsheng Ma, University of Arizona; Paul Brokaw, Analog Devices Inc

A2L-D2 **A Fully-Integrated 130 nm CMOS DC-DC Step-Down Converter,**
10.10 **Regulated by a Constant On/Off-Time Control System**
Author(s): Mike Wens, Michiel Steyaert, Katholieke Universiteit Leuven

A2L-D3 **An on-Chip Dual Supply Charge Pump System for 45nm PD SOI eDRAM**
10.30
Author(s): Jente Kuang, Abraham Mathews, John Barth, Fadi Gebara, Tuyet Nguyen, IBM; Jeremy Schaub, IBM Austin Research Lab; Kevin Nowka, Gary Carpenter, Donald Plass, Erik Nelson, Ivan Vo, William Reohr, Toshiaki Kirihata, IBM

A2L-E **Temperature and Gas Sensors**
Moorfoot
Chair(s): Andreas Demosthenous, University College, London

A2L-E1 **A Time-Domain SAR Smart Temperature Sensor with −0.25˜+0.35°C Inaccuracy for on-Chip Monitoring**
09.50
Author(s): Poki Chen, Kai-Ming Wang, Yu-Han Peng, Yu-Shin Wang, Chun-Chi Chen, National Taiwan University of Science and Technology

A2L-E2 **A Temperature-to-Digital Converter Based on an Optimized Electrothermal Filter**
10.10
Author(s): Mahdi Kashmiri, Sha Xia, Kofi Makinwa, Delft University of Technology

A2L-E3 **A Fully Integrated Interface Circuit for 1.5°C Accuracy Temperature Control and 130-dB Dynamic-Range Read-Out of MOX Gas Sensors**
10.30
Author(s) Andrea Lombardi, Marco Grassi, Luca Bruno, Piero Malcovati, University of Pavia; Andrea Baschirotto, University of Milano – Bicocca

10.50 Coffee Break

A2L-F **Delay Locked Loops**
Kilsyth
Chair(s): Doris Schmitt-Landsiedel, Technical University of Munich

A2L-F1 **A 0.17-1.4GHz Low-Jitter All Digital DLL with TDC-Based DCC Using Pulse Width Detection Scheme**
09.50
Author(s): Dongsuk Shin, Won-Joo Yun, Hyun-Woo Lee, Young-Jung Choi, Hynix Semiconductor; Suki Kim, Chulwoo Kim, Korea University

A2L-F2 **A 2 GHz 7 mW Digital DLL-Based Frequency Multiplier in 90 nm CMOS**
10.10
Author(s): Behzad Mesgarzadeh, Atila Alvandpour, Linkoping University

A2L-F3 **A 15 MHz – 600 MHz, 20 mW, 0.38 mm2, Fast Coarse Locking Digital DLL in 0.13µm CMOS**
10.30
Author(s): Sebastian Hoyos, Texas A&M University; Cheongyuen Tsang, University of California, Berkeley; Johan Vanderhaegen, Robert Bosch Corporation; Yun Chiu, University of Illinois at Urbana Champaign; Yasutoshi Aibara, Renesas Technology Corporation; Haideh Khorramabadi, Borivoje Nikolic, University of California, Berkeley

A3L-D **RF Building Block**
Tinto
Chair(s): Marc Tiebout, Infineon Technologies

A3L-D1 **A 0.042 mm² Fully Integrated Analog PLL with Stacked**

11.20 **Capacitor-Inductor in 45 nm CMOS**
Author(s): Shih-An Yu, Peter Kinget, Columbia University

A3L-D2 **A 1.7 GHz 1.5 mW Digitally-Controlled FBAR Oscillator with**
11.40 **0.03 ppb Resolution**
Author(s): Ito Hiroyuki, Tokyo Institute of Technology; Hasnain Lakdawala, Ashoke Ravi, Stefano Pellerano, Intel Corporation; Rich Ruby, Avago Technologies; Krishnamurthy Soumyanath, Intel Corporation; Kazuya Masu, Tokyo Institute of Technology

A3L-D3 **24-GHz 1-V Pseudo-Stacked Mixer with Gain-Boosting**
12.00 **Technique**
Author(s): Nobuhiro Shiramizu, Toru Masuda, Takahiro Nakamura, Hitachi, Ltd; Katsuyoshi Washio, Central Res Lab, Hitachi, Ltd

A3L-D4 **A 65-nm CMOS 8-GHz Injection Locked Oscillator for HDR**
12.20 **UWB Applications**
Author(s): Romaric Toupé, Yann Deval, IMS Laboratory; Franck Badets, STMicroelectronics; Jean-Baptiste Bégueret, IMS Laboratory

A3L-E **Unconventional Image Sensors and Circuits**
Moorfoot
Chair(s): Jed Hurwitz, Gigle Semiconductor

A3L-E1 **A 600-GHz CMOS Focal-Plane Array for Terahertz Imaging**
11.20 **Applications**
Author(s): Ullrich Pfeiffer, Erik Öjefors, University of Wuppertal

A3L-E2 **Single-Photon Synchronous Detection**
11.40
Author(s): Cristiano Niclass, Claudio Favi, Theo Kluter, Frederic Monnier, Edoardo Charbon, Ecole Polytechnique Fédérale de Lausanne

A3L-E3 **Highly Sensitive UV-Enhanced Linear CMOS Photosensor**
12.00
Author(s): Daniel Durini, Erol Özkan, Werner Brockherde, Bedrich Hosticka, Fraunhofer Institute of Microelectronic Circuits and Systems

A3L-E4 **A 3-TFT Hybrid Active-Passive Pixel with Correlated Double**
12.20 **Sampling CMOS Readout Circuit for Real-Time Medical X-Ray Imaging**
Author(s): Nader Safavian, Karim S Karim, University of Waterloo; Arokia Nathan, London Center for Nanotechnology; John A Rowlands, Sunnybrook Health Science Centre,University of Toronto

A3L-F **On-chip digital monitors and regulators**
Kilsyth
Chair(s): Per Larsson-Edefors, Chalmers University of Technology

A3L-F1 **On-Chip Jitter and Oscilloscope Circuits Using an**
11.20 **Asynchronous Sample Clock**
Author(s): Jeremy Schaub, IBM Austin Research Lab; Fadi Gebara, Tuyet Nguyen, Ivan Vo, Jarom Peña, Dhruva Achayrra, IBM

A3L-F2 **CMOS Unclonable System for Secure Authentication Based on**
11.40 **Device Variability**
Author(s): Daniele Puntin, Stefano Stanzione, Giuseppe Iannaccone,

Università di Pisa

A3L-F3 **Circuit Techniques for Suppression and Measurement of on-Chip Inductive Supply Noise**
12.00
Author(s): Sanjay Pant, AMD Inc; David Blaauw, University of Michigan

A3L-F4 **A Fully Integrated Power Supply Unit for Fine Grain Power Management Application to Embedded Low Voltage SRAMs**
12.20
Author(s): Edith Beigné, CEA LETI – MINATEC; Fabien Clermidy, Sylvain Miermont, Alexandre Valentian, Pascal Vivet, CEA; Sebastien Barasinski, Febrice Blisson, N Kholi, S Kumar, STMicroelectronics

12.50 Lunch

A4L-A **Joint plenary** V. Manian
Pentland
Chair(s): Bill Redman-White, NXP/University of Southampton
Robert Henderson, University of Edinburgh

A4L-A1 **Technology Interfacing for Fabless Semiconductor Companies**
14.10
Author(s): Vahid Manian, Broadcom

A5L-B **ESSDERC plenary** T. Hamamoto
Pentland
Chair(s): TBC

A5L-B1 **Information, Energy, and Entropy: Design Principles for Adaptive, Therapeutic Modulation of Neural Circuits**
15.00
Author(s): S Jensen, G Molnar, J Giftakis, W Santa, R Jensen, D Carlson, M Lent, Timothy Denison, Medtronic

15.40 Coffee break

A6L-D **Transceivers and Tuners**
Tinto
Chair(s): Sven Mattisson

A6L-D1 **A Single-Chip 8-Band CMOS Transceiver for W-CDMA(HSPA)/ GSM(GPRS)/EDGE with Digital Interface**
16.10
Author(s): Hiroshi Yoshida, Takehiko Toyoda, T Yasuda, Y Ogasawara, M Ishii, T Murasaki, G Takemura, M Iwanaga, T Takida, Toshiba Corporation; Yuta Araki, Toshiba Corporation Semiconductor Company; T Hashimoto, K Sami, T Imayama, H Shimizu, H Kokatsu, Toshiba Corporation

A6L-D2 **A Low Power CMOS SAW-Less Quad Band WCDMA/HSPA/1X/EGPRS Transmitter**
16.30
Author(s): Marco Cassia, Aristotele Hadjichristos, Hong Sun Kim, Jin-Su Ko, Jeongsik Yang, Sang-Oh Lee, Kamal Sahota, Qualcomm

A6L-D3 **A 14-mW 2.4-GHz CMOS Transceiver for Short Range Wireless Sensor Applications**
16.50
Author(s): Reza Yousefi, Ralph Mason, Carleton University

A6L-D4 **A Multi-Standard Mobile Digital Video Receiver in 0.18µm CMOS**
17.10

Author(s): Kenneth Barnett, Harish Muthali, Susanta Sengupta, Yunfei Feng, Bo Yang, Zhije Xiong, Tae Wook Kim, James Jaffee, Cormac Conroy, Qualcomm Inc

A6L-D5 **On-Chip Auto-Calibrated RF Tracking Filter for Cable Silicon Tuner**
17.30
Author(s): Olivier Jamin, Vincent Rambeau, Frederic Mercier, Insaf Meliane, NXP Semiconductors

A6L-E **High Speed Data Links**
Moorfoot
Chair(s): Masaru Kokubo

A6L-E1 **Power Efficient 4.5Gbit/s Optical Receiver in 130nm CMOS with ??????????????**
16.10
Author(s): Filip Tavernier, Michiel Steyaert, Katholieke Universiteit Leuven

A6L-E2 **5.75 to 44 Gb/s Quarter Rate CDR with Data Rate Selection in 90 nm Bulk CMOS**
16.30
Author(s): George von Bueren, Lucio Rodoni, Heinz Jaeckel, Electronics Laboratory, ETH Zuerich; Alex Huber, University of Applied Sciences Northwestern Switzerland; Roland Brun, Daniel Holzer, Bern University of Applied Sciences; Martin Schmatz, IBM Zurich Research Laboratory

A6L-E3 **A Robust 1.5 Gb/s + 3 Gb/s Serial PHY with Feed-Forward Correction Clock and Data Recovery**
16.50
Author(s): William Redman-White, Martin Bugbee, Steve Dobbs, Xinyan Wu, Richard Balmford, Jonah Nuttgens, Umer Kiani, Richard Clegg, Gerrit Den Besten, NXP Semiconductors

A6L-E4 **A Low-Jitter 1.5 GHz and 350 ppm Spread-Spectrum Serial ATA PHY Using Reference Clock with 400 ppm Production-Frequency Tolerance**
17.10
Author(s): Takashi Kawamoto, Hitachi, Ltd / Central Research Laboratory; Masaru Kokubo, Hitachi Ltd

AL6-E5 **An Adaptive 4-Tap Analog FIR Equalizer for 10-Gb/s Over Backplane Serial Link Receiver**
17.30
Author(s): Ori Eshet, Adee Ran, Amir Mezer, Yaniv Hadar, Dror Lazar, Miki Moyal, Intel

AL6-F **Low Power Processors and Memory**
Kilsyth
Chair(s): Stefan Rusu, Intel Corporation

AL6-F1 **A 2.9Tb/s 8W 64-Core Circuit-Switched Network-on-Chip in 45 nm CMOS**
16.10
Author(s): Mark Anders, Himanshu Kaul, Martin Hansson, Ram Krishnamurthy, Shekhar Borkar, Intel Corporation

AL6-F2 **Standby Power Reduction Techniques for Ultra-Low Power Processors**
16.30
Author(s): Yoonmyung Lee, University of Michigan; Mingoo Seok, University of Michigan Ann Arbor; Scott Hanson, David Blaauw, Dennis Sylvester, University of Michigan

AL6-F3 **Low-Power 32-Bit Dual-MAC 120 µW/MHz 1.0 V icyflex DSP/MCU Core**
16.50
Author(s): Claude Arm, Stève Gyger, Jean-Marc Masgonty, Marc Morgan, Jean-Luc Nagel, Christian Piguet, Flavio Rampogna, Patrick Volet, Swiss Center for Electronics and Microtechnology

AL6-F4 **A 5.2Gb/p/s GDDR5 SDRAM with CML Clock Distribution Network**
17.10
Author(s): Kyung Hoon Kim, Sangsic Yoon, Kichang Kwean, Daehan Kwon, Sunsuk Yang, Munphil Park, Yongki Kim, Byongtae Chung, Hynix Semiconductor Inc

AL6-F5 **Program Circuit for a Phase Change Memory Array with 2 MB/s Write Throughput for Embedded Applications**
17.30
Author(s): Guido De Sandre, Luca Bettini, Emanuela Calvetti, Gianni Giacomi, Marco Pasotti, Massimo Borghi, Paola Zuliani, Roberto Annunziata, STMicroelectronics; Innocenzo Tortorelli, Fabio Pellizzer, Roberto Bez, ST M6 SRL

Wednesday September 17

B1L-A **Joint plenary** C. Van Hoof
Pentland
Chair(s): Stephen Hall, University of Liverpool
Peter Ashburn, University of Southampton

B1L-A1 **Micropower Energy Scavenging**
08.30
Author(s): Paolo Fiorini, Inge Doms, Chris van Hoof, Ruud Vullers, IMEC

B2L-B **ESSCIRC plenary** Y. Hagihara
Pentland
Chair(s): TBC

B2L-B1 **SOI Design in Cell Processor and Beyond**
09.30
Author(s): Yoshiaki Daimon Hagihara, AIPS/AINS Consortium

B3L-D **Oversampled Data Converters**
Tinto
Chair(s): Piero Malcovati, University of Pavia

B3L-D1 **A 3.6 GHz, 16 mW Sigma-Delta DAC for a 802.11 n/802.16 e Transmitter with 30 dB Digital Power Control in 90 nm CMOS**
10.40
Author(s): Ashoke Ravi, Intel Corp; Parmoon Seddighrad, Intel Corp/University of Washington; Masoud Sajadieh, Hasnain Lakdawala, Krishnamurthy Soumyanath, Intel Corp

B3L-D2 **A 12-bit 3.125-MHz Bandwidth 0-3 MASH Delta-Sigma Modulator**
11.00
Author(s): Ahmed Gharbiya, David Johns, University of Toronto

B3L-D3 **A 20.7 mW Continuous-Time Delta Sigma Modulator with 15 MHz Bandwidth and 70 dB Dynamic Range**
11.20
Author(s): Karthikeyan Reddy, Texas Instruments; Shanthi Pavan, Indian Institute of Technology, Madras

B3L-D4 **A 11 mW 68dB SFDR 100 MHz Bandwidth Delta-Sigma-DAC**
11.40 **Based on a 5-Bit 1 GS/s Core in 130 nm**
Author(s): Pieter Palmers, Michiel Steyaert, Katholieke Universiteit Leuven

B3L-D5 **Third-Order Sigma-Delta Modulator with 61 dB SNR and 6 MHz**
12.00 **Bandwidth Consuming 6 mW**
Author(s): Edoardo Bonizzoni, Aldo Peña Perez, Franco Maloberti, University of Pavia; Miguel Garcia-Andrade, University of Ciudad Juare

B3L-E **Memory Design Techniques** Moorfoot
Chair(s): Wim Dehaene, KULeuven-ESAT

B3L-E1 **Parallel Double Error Correcting Code Design to Mitigate**
10.40 **Multi-Bit Upsets in SRAMs**
Author(s): Riaz Naseer, University of Southern California; Jeff Draper, University of Southern California / Information Sciences Institute

B3L-E2 **A Multiword Based High Speed ECC Scheme for Low-Voltage**
11.00 **Embedded SRAMs**
Author(s): Shah Jahinuzzaman, Tahseen Shakir, Sumanjit Lubana, Jaspal Shah, Manoj Sachdev, University of Waterloo

B3L-E3 **Importance Sampling Monte Carlo Simulations for Accurate**
11.20 **Estimation of SRAM Yield**
Author(s): Toby Doorn, Jan Ter Maten, NXP Semiconductors; Jeroen Croon, NXP-TSMC Research Center; Alessandro Di Bucchianico, Olaf Wittich, Eindhoven University of Technology

B3L-E4 **A Robust Single Supply Voltage SRAM Read Assist Technique**
11.40 **Using Selective Precharge**
Author(s): Mohamed Abu-Rahma, Qualcomm Incorporated; Mohab Anis, University of Waterloo; Sei Seung Yoon, Qualcomm Incorporated

B3L-E5 **A 45 nm Single Power Supply SRAM Supporting Low Voltage**
12.00 **Operation Down to 0.6 V**
Author(s): Sebastien Barasinski, Ludovic Camus, Sylvain Clerc, STMicroelectronics

B3L-F **60 GHz and Beyond**
Kilsyth
Chair(s): Michiel Steyoert, KULeauven

B3L-F1 **A 90 nm CMOS mm-Wave VCO Using an LC Tank with Inductive**
10.40
Author(s): Lianming Li, Patrick Reynaert, Michiel Steyaert, Katholieke Universiteit Leuven

B3L-F2 **A Fully Integrated 60 GHz Transmitter Front-End with a PLL, an**
11.00 **Image-Rejection Filter and a PA in SiGe**
Author(s): Srdjan Glisic, Yaoming Sun, Frank Herzel, Maxim Piz, Eckhard Grass, Christoph Scheytt, IHP; Wolfgang Winkler, Silicon Radar GmbH

B3L-F3 **60GHz Quadrature Doppler Radar Transceiver in a 0.25 µm**
11.20 **SiGe BiCMOS Technology**
Author(s): Hugo Veenstra, Marc Notten, Philips Research Laboratories Eindhoven; Xiongchuan Huang, John Long, Delft University of

Technology

B3L-F4 **A 60GHz Digitally Controlled Phase Shifter in CMOS**
11.40
Author(s): Yikun Yu, Peter Baltus, Arthur van Roermund, Eindhoven University of Technology; Dennis Jeurissen, Anton de Graauw, Edwin van der Heijden, Ralf Pijper, NXP Semiconductors

B3L-F5 **A 71–73 GHz Voltage-Controlled Standing-Wave Oscillator in 90 nm CMOS Technology**
12.00
Author(s): Francesco De Paola, Raffaella Genesi, Danilo Manstretta, Università degli Studi di Pavia

12.20 Lunch

B4L-A **Joint plenary** T.Sakurai
Pentland
Chair(s): TBC

B4L-A1 **Solving Issues of Integrated Circuits by 3D-Stacking Meeting with the Era of Power, Integrity Attackers and NRE Explosion and a Bit of Future**
13.50
Author(s): Takayasu Sakurai, University of Tokyo

B5L-A **Process Stability** Joint session
Pentland
Chair(s): Asen Asenov, University of Glasgow

B5L-A1 **On-Chip Leakage Monitor Circuit to Scan Optimal Reverse Bias Voltage for Adaptive Body-Bias Circuit Under Gate Induced Drain Leakage Effect**
14.40
Author(s): Masako Fujii, Hiroaki Suzuki, Hiromi Notani, Hiroshi Makino, Hirofumi Shinohara, Renesas Tech Corp

B5L-A2 **Impact of Strain on LER Variability in bulk MOSFETs**
15.00
Author(s): Xingsheng Wang, Scott Roy, Asen Asenov, University of Glasgow

B5L-A3 **On the Stability of Fully Depleted SOI MOSFETs Under Lithography Process Variations**
15.20
Author(s): Christian Kampen, Tim Fühner, Alexander Burenkov, Andreas Erdmann, Heiner Ryssel, Fraunhofer Institute of Integrated Systems and Device Technology

B5L-D **Nyquist Rate Data Converters**
Tinto
Chair(s): Klaas Bult, Broadcom

B5L-D1 **A 1.5V 13bit 130-300MS/s Self-calibrated DAC with Active Output Stage and 50MHz Signal Bandwidth in 0.13 µm CMOS**
14.40
Author(s): Martin Clara, Wolfgang Klatzer, Daniel Gruber, Arnold Marak, Berthold Seger, Infineon Technologies AG; Wolfgang Pribyl, Graz University of Technology

B5L-D2 **A 90 nm 8 b 120 Ms/s-250 Ms/s Pipeline ADC**
15.00
Author(s): Luca Picolli, Piero Malcovati, University of Pavia; Lorenzo Crespi,

Faouzi Chaahoub, Conexant; Andrea Baschirotto, University of Milano - Bicocca

B5L-D3 15.20 **A 1.2V 56mW 10 Bit 165Ms/s Pipeline-ADC for HD-Video Applications**
Author(s): Martin Trojer, Mauro Cleris, Ulrich Gaier, Thomas Hebein, Peter Pridnig, Bernhard Kuttin, Bernhard Tschuden, Christian Krassnitzer, Christian Kuttin, Micronas Villach; Wolfgang Pribyl, Graz University of Technology

B5L-D4 15.40 **An 8-Bit Flash Analog-to-Digital Converter in Standard CMOS Technology Functional in Ultra Wide Temperature Range from 4.2 K to 300 K**
Author(s): Ybe Creten, Patrick Merken, Robert Mertens, IMEC; Willy Sansen, Katholieke Universiteit Leuven; Chris van Hoof, IMEC

B5L-E Moorfoot **Low Power SRAM**
Chair(s): Tobias Noll, RWTH Aachen University

B5L-E1 14.40 **A 3.6 pJ/Access 480 MHz, 128 Kbit on-Chip SRAM with 850 MHz Boost Mode in 90 nm CMOS with Tunable Sense Amplifiers to Cope with Variability**
Author(s): Stefan Cosemans, Wim Dehaene, Katholieke Universiteit Leuven; Francky Catthoor, IMEC

B5L-E2 15.00 **A Reconfigurable 65 nm SRAM Achieving Voltage Scalability from 0.25–1.2 V and Performance Scalability from 20 kHz-200 MHz**
Author(s): Mahmut Sinangil, Naveen Verma, Anantha Chandrakasan, Massachusetts Institute of Technology

B5L-E3 15.20 **A Cell-Activation-Time Controlled SRAM for Low-Voltage Operation in DVFS SoCs Using Dynamic Stability Analysis**
Author(s): Masanao Yamaoka, Kenichi Osada, Takayuki Kawahara, Hitachi, Ltd

B5L-E4 15.40 **A Dual Port Dual Width 90 nm SRAM with Guaranteed Data Retention at Minimal Standby Supply Voltage**
Author(s): Peter Geens, Wim Dehaene, Katholieke Universiteit Leuven

B5L-F Kilsyth **Circuit Techniques for UWB**
Chair(s): Jan Craninckx, IMEC

B5L-F1 14.40 **Current Reuse CMOS LNA for UWB Applications**
Author(s): Thierry Taris, Yann Deaal, Jean Baptiste Bégueret, IMS Laboratory

B5L-F2 15.00 **A UWB Transformer-C Orthonormal State Space Band-Reject Filter in 0.13 µm CMOS**
Author(s): Sumit Bagga, Zoubir Irahhauten, Delft University of Technology; Sandro Haddad, Freescale Semiconductores Brazil; Wouter Serdijn, John Long, Delft University of Technology; John Pekarik, IBM Microelectronics

B5L-F3 **A 9mW High Band FM-UWB Receiver Front-End**

15.20
Author(s): Yunzhi Dong, Yi Zhao, John Gerrits, Delft University of Technology; Gerrit Veenendaal, IC Lab, NXP Semiconductors; John Long, Delft University of Technology

B5L-F4 **A Low-Voltage Mobility-Based Frequency Reference for Crystal**
15.40 **Less ULP Radios**

16.00 Coffee break

B6L-D **Amplifiers**
Tinto
Chair(s): Marco Berkhout, NXP

B6L-D1 **A 36 V Precision Programmable Gain Amplifier with CMRR**
16.30 **Exceeding 120 dB in All Gains**
Author(s): Viola Schaffer, Martijn Snoeij, Misha Ivanov, Texas Instruments GmbH

B6L-D2 **A 65-nm 84-dB-Gain 200-MHz-UGB CMOS Fully-Differential**
16.50 **Three- Stage Amplifier with a Novel Common Mode Control**
Author(s): Ivonne Di Sancarlo, University of Salento; Dario Giotta, Infineon Technologies AG; Andrea Baschirotto, University of Milano – Bicocca; Richard Gaggl, Infineon Technologies AG

B6L-D3 **A CMOS Source-Buffered Differential Input Stage with High EMI Suppression**
17.10
Author(s): Jean-Michel Redouté, Michiel Steyaert, Katholieke Universiteit Leuven

B6L-D4 **Analog Signal Processing for a Class D Audio Amplifier in**
17.30 **65 nm CMOS Technology**
Author(s): Willem Groeneweg, NXP Semiconductors
B6L-E Components in High Frequency Circuits
Moorfoot
Chair(s): Harold Gamble, Queens University Belfast

B6L-E1 **High Efficiency Embedded Decoupling Capacitors for MCM**
16.30 **Applications**
Author(s): Olivier Tesson, François Le Cornec, Sebastien Jacqueline, NXP Semiconductors

B6L-E2 **Reduction of Low-Frequency Noise in MOSFETs Under**
16.50 **Switched Gate and Substrate Bias**
Author(s): Domagoj Siprak, Infineon Technologies AG; Nicola Zanolla, University of Bologna; Marc Tiebout, Infineon Technologies AG; Peter Baumgartner, Infineon Technologies AG, Claudio Fiegna, University of Bologna

B6L-E3 **Reduction of VCO Phase Noise Through Forward Substrate**
17.10 **Biasing of Switched MOSFETs**
Author(s): Domagoj Siprak, Marc Tiebout, Peter Baumgartner, Infineon Technologies AG

B6L-F **UWB TX Synthesisers**
Kilsyth

Chair(s): Giuseppe Gramegna, Cambridge Silicon Radio

B6L-F1 **A WiMedia UWB Receiver with a Synthesizer**
16.30
Author(s): Mikko Kaltiokallio, Helsinki University of Technology; Ville Saari, Tapio Rapinoja, Kari Stadius, Jussi Ryynänen, Saska Lindfors, Kari Halonen, Helsinki University of Technology / Electronic Circuit Design Laboratory / TKK

B6L-F2 **An Ultra Low Power and High Efficiency UWB Transmitter for WPAN Applications**
16.50
Author(s): Shengxi Diao, Yuan Jin Zheng, Institute of Microelectronics

B6L-F3 **A 3-10 GHz Flexible CMOS LO Generator for MB-OFDM UWB Application Using Wide Tunable VCOs**
17.10
Author(s): Eun-Chul Park, Inhyo Ryu, Jeongwook Koh, Chun-Deok Suh, Samsung Electronics Co

B6L-F4 **0.13 µm CMOS Cartesian Loop Transmitter IC with Fast Calibration and Switching Scheme from Opened to Closed Loop**
17.30
Author(s): Shoji Otaka, Corporate Reserch and Development Center, Toshiba Corporation; Masahiro Hosoya, Hiroaki Ishihara, Toshiba Corporation; Toru Hashimoto, Semiconductor Company, Toshiba Corporation; Yuta Araki, Toshiba Corporation Semiconductor Company

Thursday 18 September

C1L-A **Joint plenary** M. Thompson
Pentland
Chair(s): Peter Mole, Intersil

C1L-A1 **More Than Moore and More Moore in Europe**
08.30
Author(s): Michael Thompson, STMicroelectronics

C2L-D **Regulators and Drivers**
Tinto
Chair(s): Wolfgang Pribyl, Graz University of Technology

C2L-D1 **Low Drop-Out Voltage Regulator with Full on-Chip Capacitance for Slot-Based Operation**
09.30
Author(s): Wim Kruiskamp, René Beumer, SiTel Semiconductor

C2L-D2 **High-Performance Low-Dropout Regulator Achieved by Fast Transient Mechanism**
09.50
Author(s): Hong-Wei Huang, RichTek Technology Corporation; Chia-Hsiang Lin, Ke-Horng Chen, National Chiao Tung University

C2L-D3 **A High-Power-Led Driver with Power-Efficient Led-Current Sensing Circuit**
10.10
Author(s): Wing Yan Leung, Tsz Yin Man, Mansun Chan, Hong Kong University of Science & Technology

C2L-D4 **Boost DC-DC Converter with Charge-Recycling (CR) and Fast Reference Tracking (FRT) Techniques for High-Efficiency and**

Low-Cost Led Driver
Author(s): Chun-Yu Hsieh, Ke-Horng Chen, National Chiao Tung University

C2L-E **Synthesis and PLLs**
Moorfoot
Chair(s): Rudolf Koch, Infineon

C2L-E1 **An 11-Bit 8.6 GHz Direct Digital Synthesizer MMIC with 10-Bit Segmented Nonlinear DAC**
09.30
Author(s): Xueyang Geng, Xuefeng Yu, Fa Foster Dai, J David Irwin, Richard Jaeger, Auburn University

C2L-E2 **Fully Integrated, High Performance Triple SD PLL (2.2 GHz to 4.4 GHz) with Minimized Interaction**
09.50
Author(s): Stefano Cipriani, Eric Duvivier, Gianni Puccio, Lorenzo Carpineto, Biagio Bisanti, Francesco Coppola, Martin Alderton, Jeremy Goldblatt, Entropic Communications

C2L-E3 **A Low-Power Programmable Dynamic Frequency Divider**
10.10
Author(s): Jérémie Chabloz, David Ruffieux, Christian Enz, Swiss Center for Electronics and Microtechnology

C2L-E4 **Supply-Noise Mitigation Techniques in Phase-Locked Loops**
10.30
Author(s): Abhijith Arakali, Oregon State University; Nema Talebbeydokthi, Intel Corporation; Srikanth Gondi, Kawasaki Microelectronics America, Inc; Pavan Kumar, Oregon State University

C2L-F **Impulse UWB Receivers**
Kilsyth
Chair(s): Kari Halonen, Helsinki University of Technology

C2L-F1 **A 46 pJ/Pulse Analog Front-End in 130 nm CMOS for UWB Impulse Radio Receivers**
09.30
Author(s): Nick Van Helleputte, Georges Gielen, Katholieke Universiteit Leuven

C2L-F2 **A 7.5 mA 500 MHz UWB Receiver Based on Super-Regenerative Principle**
09.50
Author(s): Prakash Egambaram Thoppay, Catherine Dehollain, Michel Declercq, Ecole Polytechnique Fédérale de Lausanne

C2L-F3 **Low-Power CMOS RF Front-End for Non-Coherent IR-UWB Receiver**
10.10
Author(s): Yuan Gao, Yuan Jin Zheng, Institute of Microelectronics; Chun-Huat Heng, National University of Singapore

C2L-F4 **Super-Regenerative UWB Impulse Detector with Synchronized Quenching Mechanism**
10.30
Author(s): Muhammad Anis, Rienhard Tielert, Norbert When, TU Kaiserslautern

10.50 Coffee break

C3L- D **Low-Power Analogue**
Tinto

Chair(s): Ralf Brederlow, Texas Instruments Deutschland GmbH

C3L-D1 11.20 **A Fully-Integrated Wienbridge Topology for Ultra-Low-Power 86 ppm/°C 65 nm CMOS 6 MHz Clock Reference with Amplitude Regulation**
Author(s): Valentijn De Smedt, Pieter De Wit, Wim Vereecken, Michiel Steyaert, Katholieke Universiteit Leuven

C3L-D2 11.40 **A 0.3 µW, 7 ppm/°C CMOS Voltage Reference Circuit for on-Chip Process Monitoring in Analog Circuits**
Author(s): Ken Ueno, Hokkaido University; Tetsuya Hirose, Kobe University; Tetsuya Asai, Yoshihito Amemiya, Hokkaido University

C3L-D3 12.00 **Electronic Interface for Piezoelectric Energy Scavenging System**
Author(s): Enrico Dallago, Daniele Miatton, Giuseppe Venchi, University of Pavia; Valeria Bottarel, STMicroelectronics; Giovanni Frattini, National Semiconductor SRL, Giulio Ricotti, Monica Schipani, STMicroelectronics

C3L-D4 12.20 **A 0.2 V–1.2 V Converter for Power Harvesting Applications**
Author(s): Anna Richelli, Luigi Colalongo, Università degli Studi di Brescia; Silvia Tonoli, University of Brescia; Zsolt Miklos Kovacs Vajna, Università degli Studi di Brescia

C3L-E Moorfoot **Multi-Standard RF**
Chair(s): Peter Kennedy, University College Cork

C3L-E1 11.20 **A Low-Complexity, Low Phase Noise, Low-Voltage Phase-Aligned Ring Oscillator in 90 nm Digital CMOS**
Author(s): Jonathan Borremans, IMEC/Vrije Universiteit Brussel; Julien Ryckaert, Piet Wambacq, IMEC; Maarten Kuijk, Vrije Universiteit Brussel; Jan Craninckx, IMEC

C3L-E2 11.40 **A 1.2 V Receiver Front-End for Multi-Standard Wireless Applications in 65 nm CMOS LP**
Author(s): Maja Vidojkovic, Eindhoven University of Technology; Mihai Sanduleanu, IMEC; Vojkan Vidojkovic, SiTel Semiconductor; Johan van der Tang, Broadcom; Peter Baltus, Arthur van Roermund, Eindhoven University of Technology

C3L-E3 12.00 **A 1.2 GHz Semi-Digital Reconfigurable FIR Bandpass Filter with Passive Power Combiner**
Author(s): Axel Flament, Antoine Frappé, Andreas Kaiser, Bruno Stefanelli, IEMN; Andreia Cathelin, Hilal Ezzeddine, STMicroelectronics

C3L-E4 12.20 **A Fractional Spur Reduction Technique for RF TDC-Based All Digital PLLs**
Author(s): Ping-Ying Wang, Hsiang-Hui Chang, Jing-Hong Conan Zhan, Mediatek

C3L-F Kilsyth **Short Range Low Data Rate Wireless Communications**
Chair(s): Christian Enz, CSEM

C3L-F1 **An Ultra Low Power SoC for 2.4 GHz IEEE802.15.4 Wireless Communications**
11.20
Author(s): Carolynn Bernier, Frédéric Hameau, CEA LETI; Gérard Billiot, CEA LETI – MINATEC; Emeric de Foucauld, Stéphanie Robinet, Didier Lattard, Jean Durupt, François Dehmas, Laurent Ouvry, Pierre Vincent, CEA LETI

C3L-F2 **A 0.23 Mm² Free Coil ZigBee Receiver Based on a Bond-Wire Self-Oscillating Mixer**
11.40
Author(s): Marika Tedeschi, Antonio Liscidini, Rinaldo Castello, Università degli Studi di Pavia

C3L-F3 **An Ultra Low Power GFSK Demodulator for Wireless Body Area Network**
12.00
Author(s): Dong Han, Yuan Jin Zheng, Institute of Microelectronics

C3L-F4 **A 3–5 GHz Low-Complexity Ultra-Wideband CMOS RF Front-End for Low Data-Rate WPANs**
12.20
Author(s): Marco Cavallaro, Alessandro Italia, Giuseppina Sapone, Giuseppe Palmisano, Università di Catania

12.40 Lunch

C4L-A **Joint plenary** V. Subramanian
Pentland
Chair(s): Roland Thewes, Qimonda
Ralf Brederlow, Texas Instruments Deutschland GmbH

C4L-A1 **Printed Electronics for Low-Cost Electronic Systems: Technology Status and Application Development**
14.10
Author(s): Vivek Subramanian, Josephine Chang, Alejandro de la Fuente Vornbrock, Daniel Huang, Lakshmi Jagannathan, Frank Liao, Brian Mattis, Steve Molesa, David Redinger, Daniel Soltman, Steven Volkman, Qintao Zhang, University of California, Berkeley

C5L-B **ESSCIRC plenary** Marco Berkhout
Pentland
Chair(s): TBC

C5L-B1 **Audio at Low and High Power**
15.00
Author(s): Marco Berkhout, Lucien Breems, NXP Semiconductors; Ed van Tuijl, Axiom IC

15.40 Coffee break

C6L-D **Sensor Interface Circuits**
Tinto
Chair(s): Kofi Makinwa, Delft University of Technology

C6L-D1 **A 828 µW 1.8 V 80 dB Dynamic-Range Readout Interface for a MEMS Capacitive Microphone**
16.10
Author(s): Syed Arsalan Jawed, IRST - Fondazione Bruno Kessler; Davide Cattin, University of Trento; Massimo Gottardi, Nicola Massari, Fondazione Bruno Kessler; Andrea Baschirotto, University of Milano – Bicocca; Andrea Simoni, Fondazione Bruno Kessler

C6L-D2 **A Low-Power Capacitance to Pulse Width Converter for MEMS Interfacing**
16.30
Author(s): Paolo Bruschi, Nicolo Nizza, Michele Dei, University of Pisa

C6L-D3 **A 14-Bit Micro-Watt Power Scalable Automotive MEMS Pressure Sensor Interface**
16.50
Author(s): Akram Nafee, David Johns, University of Toronto

C6L-D4 **A High Gain-Bandwidth Product Transimpedance Amplifier for MEMS-Based Oscillators**
17.10
Author(s): Frederic Nabki, Mourad El-Gamal, McGill University

C6L-D5 **A Synchronous Chopping Technique and Implementation for High-Frequency Precision Sensing**
17.30
Author(s): Mohamad Rahal, Andreas Demosthenous, University College London

C6L-E **High-Speed Digital Circuits and Systems**
Moorfoot
Chair(s): Hannu Tenhunen

C6L-E1 **A 211 GOPS/W Dual-Mode Real-Time Object Recognition Processor with Network-on-Chip**
16.10
Author(s): Kwanho Kim, Joo-Young Kim, Seungjin Lee, Minsu Kim, Hoi-Jun Yoo, Korea Advanced Institute of Science and Technology

C6L-E2 **A Fully Programmable 40 GOPS SDR Single Chip Baseband for LTE/WiMAX Terminals**
16.30
Author(s): Torsten Limberg, Markus Winter, Marcel Bimberg, Reimund Klemm, Emil Matus, Marcos Tavares, Gerhard Fettweis, Hendrik Ahlendorf, Pablo Robelly, TU Dresden

C6L-E3 **2.6 Gb/s Over a Four-Drop Bus Using an Adaptive 12-Tap DFE**
16.50
Author(s): Henrik Fredriksson, Christer Svensson, Linköping University

C6L-E4 **An 8Gbps 2.5 mW on-Chip Pulsed-Current-Mode Transmission Line Interconnect with a Stacked-Switch Tx**
17.10
Author(s): Tomoaki Maekawa, Integrated Research Institute, Tokyo Institute of Technology; Hiroyuki Ito, Tokyo Institute of Technology; Kazuya Masu, Integrated Research Institute, Tokyo Institute of Technology

C6L-E5 **Implementation of a Phase-Encoding Signalling Prototype Chip**
17.30
Author(s): Crescenzo D'Alessandro, Alex Bystrov, Alex Yakovlev, Newcastle University

C6L-F **RF Power Amplifiers and Radar**
Kilsyth
Chair(s): Braum Nauta, University of Twente

C6L-F1 **A High-Resolution 24 dBm Digitally-Controlled CMOS PA for Multi-Standard RF Polar Transmitters**
16.10
Author(s): Calogero Davide Presti, Francesco Carrara, Giuseppe Palmisano, Università di Catania; Antonino Scuderi, STMicroelectronics Catania

C6L-F2 **A 1.2 V, 17 dBm Digital Polar CMOS PA with Transformer-Based Power Interpolating**
16.30
Author(s): Xin He, Manel Collados, Nenad Pavlovic, Jan van Sinderen, NXP Semiconductors

C6L-F3 **A 2.4 GHz +25 dBm P-1 dB Linear Power Amplifier with Dynamic Bias Control in a 65 nm CMOS Process**
16.50
Author(s): Po-Chih Wang, Kai-Yi Huang, Yu-Fu Kuo, Ming-Chong Huang, Chao-Hua Lu, Tzung-Ming Chen, Chia-Jun Chang, Ka-Un Chan, Ta-Hsun Yeh, Wen-Shan Wang, Ying-His Lin, Chao-Cheng Lee, Realtek Semiconductor Corp

C6L-F4 **0.13 µm SiGe BiCMOS Radio Front-End Circuits for 24 GHz Automotive Short-Range Radar Sensors**
17.10
Author(s): Angelo Scuderi, STMicroelectronics, Automotive Product Group, RF Competence Center; Egidio Ragonese, Giuseppe Palmisano, Università di Catania

C6L-F5 **A 24 GHz FMCW Radar Transmitter in 0.13 µm CMOS**
17.30
Author(s): Yiqun Cao, Marc Tiebout, Infineon Technologies AG; Vadim Issakov, Universitiy of Paderborn / Infineon Technologies AG

ESSCIRC workshops

WS 1 CMOS Variability Research in Europe: From Atomic Scale to Circuits and Systems

The increasing variability in CMOS transistor characteristics has become a major challenge to scaling and integration. Statistical variability related to the fundamental discreteness of charge and matter, which cannot be eliminated by tighter process control, is becoming the major component of CMOS variability. The increasing device variability demands fundamental changes in the way that future integrated circuits and systems are designed. Strong links must be established between circuit design, system design and fundamental device technology to allow circuits and systems to accommodate the individual behaviour of every transistor on a chip. Design paradigms must change to accommodate the increasing variability. This workshop presents the status of CMOS variability related research in Europe conducted in three European and two national projects, including:

NANOSIL Silicon-based nanostructures and nanodevices for long-term nanoelectronics applications (EU FP7)
PULLNANO Pulling the limits of nanoCMOS Electronics (EU FP6)-
REALITY Reliable and variability tolerant system-on-a-chip design in More-Moore technologies (EU FP7)-
NanoCMOS Meeting the design challenges of nanoCMOS electronics (UK EPSRC)-
NanoMat Meeting the material challenges of nanoCMOS electronics (UK EPSRC)-

The workshop covers a broad range of technology, devices, and design aspects of the CMOS variability from atomic scale to circuit and system level. The keynote speaker, Prof. Toshiro Hiramoto from Tokyo University, will introduce the subject and will present the concerted research effort, supported by the MIRAI Project in Japan, in characterising and understanding the sources of statistical CMOS variability.

Agenda

09.00	**Welcome and introduction** A. Ionescu, EPFL, Switzerland
09.10	**Measuring and Understanding Device Variability** Keynote, T. Hiramoto, Tokyo University (MIRAI)
09.40	**Link Between 'Ab Initio' Material Simulation and Variability** A. Shuger, UCL (NanoMAT)
10.10	**Simulation of Statistical Variability Introduced by Discreteness of Charge and Matter** A. Asenov, University of Glasgow (NanoMAT)
10.40	Coffee break
11.00	**Measuring and Simulation of STMicroelectronics/Device Variability at 45 nm Technology Generation** A. Cathignol, IMEP

11.30	**Measurement and Simulation of Statistical Variability in FinFETS** A. Mercha, IMEC (PULLNANO)
12.00	**Variability in Novel Device Architectures** G. Iannaccone, IU.NET (NANOSIL)
12.30	Lunch
13.30	**Reliable and Variability-Tolerant System-on-Chip Design Strategies** B. Dierickx & M. Miranda, IMEC (REALITY)
14.00	**Grid Technology to Support Statistical Device and Circuit Simulation** S. Roy, University of Glasgow (NanoCMOS)
14.30	**Impact of Variability on Multicore Processor Architectures** S. Furber, Manchester University (NanoCMOS)
15.00	**Hardware-Software Interactions in Variability and Reliability Aware Design** L. Benini, University of Bologna (REALITY)
15.30	Coffee break
16.00	**Brainstorming Session: Practical Solution for Variability Resistant Devices, Circuits and Systems** A. Shluger, A. Asenov, G. Ghibaudo, S. Furber, B. Dierickx, industry representatives
17.00	End of workshop

WS 2 Electronic cubes: a More-than-Moore platform for Wireless Sensor Nodes exploiting the 3rd Dimension

Agenda

09.00	**Opening and Short Introduction** A. Ionescu, EPFL, Switzerland
09.15	**Morphic Architectures: Atomic-Level Limits (10 μm cube)** (KEYNOTE) Ralph Cavin, Semiconductor Research Corporation, Reasearch Triangle Park, USA
09.45	**Overview of Integrated Project e-CUBES** Werner Weber, Infineon, Germany
10.15	Coffee break
10.45	**e-CUBES 3D Integration Technologies** Thierry Hilt, CEA, France
11.15	**e-CUBES Functional Blocks for 3D Integration** TBD
11.45	**Overview of MINAmI Project: Towards Ambient Intelligence for Everyday Life** (INVITED) Pascal Ancey, Industry Representatives STMicroelectronics, France
12.15	Lunch
14.00	**Energy Scavenging Research at the University of Southampton** (INVITED) Stephen Beeby, University of Southampton, UK

14.30	**Overview of Project NANOPACK** (INVITED) Afshin Ziaei, Thales, France
15.00	**Wireless Sensor Networks for Space** TBD, EPFL, Switzerland
15.30	End of workshop

WS 3 Workshop on Germanium and III-V MOS Technology

The time when technology-driven dimensional scaling could provide simultaneously high-density/low cost and high performance circuits is over. Further scaling does not guarantee performance benefits. From now on, novel device architectures and new materials may be necessary to obtain the required performance. In fact, Hf-based dielectric/metal gate combinations have replaced the long standing SiO_2/polysilicon in the gate of transistors. The new gates are already in production for the 45 nm CMOS since the end of 2007 by leading ICs manufacturer. What is next? Some people believe that new high mobility channels such as germanium and III-V compounds may be needed for future device generations.

In this workshop experts from academia, technology development laboratories and semiconductor manufacturers will come together to discuss the challenges toward a viable high mobility MOS technology. The experts will describe large scale initiatives in the US, Asia and Europe and they will introduce the main issues which will be subsequently debated in two panel discussions.

In the first morning session we will address issues related to gate dielectric and device architecture and performance. At the end, during the panel discussion we will try to answer a few difficult questions. Is it feasible to develop a complementary MOS technology which will be based entirely on Germanium? The answer to this question is not easy at the present time. We can only say that Ge CMOS is highly desirable because it simplifies processing. The main obstacle is that Ge nMOSFETs do not work as expected and we do not know why. Is this problem related to materials and/or device processing or is it of more fundamental nature related to the semiconductor itself? In the case of III-V MOSFETs, the problems are even more difficult to solve. The consensus is that a high density of defect states, probably near midgap, pin the Fermi level, thus inhibiting inversion in GaAs.

Which is the best way to passivate the GaAs surface? Which is the best device architecture and operation mode? Is it better to go for surface inversion-type with implanted S/D or buried channel implant-free devices? Is InGaAs channel better than GaAs and why?

While high mobility channels show advantage over Si in discrete long channel research devices, the situation becomes unclear when dimensions shrink. Will mobility retain high values or will it degrade as in the case of Si nanoscaled devices? More importantly, is mobility a relevant physical quantity at nanoscale dimensions or perhaps quasi-ballistic transport sets new rules for the on-state current and performance in general? Will the off-state current be under control especially for Ge devices which are expected to suffer from band-to-band tunneling?

During the second session in the afternoon and in the panel discussion at the end we will address integration issues including heteroepitaxy and engineered substrates, self-aligned processing, junctions and contacts. As it looks right

now, Ge performs well for pMOS only while III-V compounds are good for nMOS, therefore Ge and III-V compounds are not competing materials; rather, they could complement each other to form a dual-channel CMOS, provided that a good co-integration scheme can be found. Which will be the best starting substrate, plain Si or GeOI? Do we have good solutions for the problems associated with heteroepitaxial growth of III-V compounds on Ge or Si? Is dual-channel Ge/III-V better than Ge/s-Si counterpart? Do we know how to process III-Vs in a self-aligned way to guarantee scaling to very small dimensions? After all, is high mobility dual-channel CMOS scalable and manufacturable so that it could be a viable technology for volume production?

Session 1: Gate materials and devices

Agenda

09.00	**Overview of Advanced High Mobility/High Velocity Research Devices** D. Antoniadis, MIT
09.20	**Device Architecture and Processing for III-V MOS Technology** M. Rodwell, UCSB
09.40	**Devices for High Performance CMOS** S. Takagi, University of Tokyo
10.00	Coffee break
10.20	**Nanoscale Ge and III-V FETs** T. Krishnamohan, Intel/Stanford University
10.40	**GaGdO and Al2O3- Passivated II-V MOSFETs** M. Hong Nat, Tsing Hua University
11.00	**A -Si-Passivated III-V MOSFETs** J. Fompeyrine, IBM-Zurich Res. Lab
11.20	**Panel Discussion 1 Speakers Session 1: Moderator A. Dimoulas**
12.00	Lunch

Session 2: Substrates and Integration

Agenda

13.30	**Ge-on-Nothing for Ultrathin Ge Microelectronics Film Integration** T. Skotnicki, ST
13.50	**GeOI/sSOI for Co-Inegration of s-Ge pMOS with s-Si nMOS** L. Clavelier, CEA-LETI
14.10	**Sub-100 nm Ge pMOS Using Si-Compatible Process Flow** M. Heyns IMEC
14.30	**Co-Integration of Ge pMOS with III-V nMOS for Heterogeneous**
14.50	**Process Modules for Implant-Free III-V MOSFETs** I. Thayne U.

	Glasgow
15.10	**Panel Discussion 2 Speakers Session 2: Moderator A. Dimoulas**
15.50	End of workshop

WS 4 MOS-AK: Towards Nano Compact Modeling Compact Modeling and Transistor Level Optimization in Analog Designs for Nano CMOS/SOI Technologies

MOS-AK Workshop on compact modelling, organised for sixth subsequent time as an integral part of the ESSDERC/ESSCIRC conference, aims to strengthen a network and discussion forum among experts in the field, create an open platform for information exchange related to compact/spice modelling, bring people in the compact modelling field together, as well as obtain feedback from technology developers, circuit designers, and CAD tool vendors. The topics cover all important aspects of compact model development, implementation, deployment and standardisation within the main theme - compact models for mainstream CMOS/SOI circuit simulation. The specific workshop goal will be to classify the most important directions for the future development of the compact models and to clearly identify areas that need further research. This workshop is designed for device process engineers (CMOS, SOI, BiCMOS, SiGe) who are interested in device modelling; ICs designers (RF/IF/analogue/mixed-Signal/SoC) and those starting in that area as well as device characterisation, modelling and parameter extraction engineers. The content will be beneficial for anyone who needs to learn what is really behind IC simulation in modern device models. The technical program of MOS-AK workshop consists of one day of tutorials given by noted academic and industry experts, also a posters session is foreseen which will be dedicated but not limited to the VHDL-AMS/Verilog-A model standardisation: http://www.mos-ak.org/edinburgh

Transistor Level Optimization in Analog Designs David M. Binkley, UNC Charlotte

Aspects of high-frequency modelling of MOSFETs with EKV3 Matthias Bucher, TUC

Transistor Modeling for Low-Power and RF IC Designs Christian Enz, CSEM

Compact modeling techniques in thin-film SOI MOSFETs Benjamin Iniguez, URV

High-level modelling and performance optimisation of mixed-technology energy harvester systems Tom J. Kazmierski, University of Southampton

LDMOS Model Benchmark for HiSIM LDMOS, MM20 and BSIM3v3 Sub-circuit Ehrenfried Seebacher, austriamicrosystems

Compact model challenges of 65nm RF-CMOS technology Sadayuki Yoshitomi, TOSHIBA

Agenda

09.00	Oral presentations

10.00	Coffee break
10.30	Oral presentations
11.30	Posters
12.00	Lunch
13.00	Oral presentations
14.30	Coffee break
15.00	Oral presentations
16.00	End of workshop

WS 5 BIES: Brain-Inspired Electronic Systems

Significant research has focused on the development of neural networks (NNs) models that can be implemented in hardware and used to inspire new techniques for real time computations.

However, there exist several fundamental bottlenecks that restrict the progress towards biological scale networks in hardware: power consumption, compactness of neuron cells and interconnect, off vs. on chip training, etc. A workshop, held on 19 September at ESSCIRC/ESSDERC08, has the aim of bringing together researchers to discuss issues related to the development of novel hardware platforms for Brain-Inspired Electronic Systems. The workshop will provide an opportunity for researchers focusing on various aspects of such systems, such as hardware implementation of spiking neurons and the associated networks, to discuss and compare different approaches to the realisation of large-scale platforms. In particular, we would like the session to draw on the expertise of researchers to provide a discussion platform on many issues related to this domain. Also the workshop will provide an opportunity to discuss applications of brain-inspired electronic systems: for example, fault tolerant computational systems.

Agenda

09.00	**Introduction and Overview: Brain-Inspired Electronic Systems and the Electronics Knowledge Transfer Network** D. Dearing, Technology Business Manager, Electronics-KTN, UK; W. Luk, Imperial College London, UK
10.00	**Coffee, posters and networking:** interested delegates are encouraged to present a poster to promote their research
10.45	**An overview of neuromorphic circuit research at ETH** Giacomo Indiveri, ETHZ, Switzerland
11.15	**Circuit design for biologically plausible neural models** Piotr Dudek, University of Manchester, UK
11.55	**Neuromorphic Computation and Control: Bio-Inspired Systems** Leena Patel/Alan Murray, University of Edinburgh, UK

12.15 Networking lunch

13.30 **Abstracting Both Architecture and Time: The SpiNNaker Neuromimetic Modelling Platform** A. Rast, S. Furber, D. Lester, S. Temple, L. Plana, E. Painkras, M. Khan, J. Wu, Y. Shi, S. Yang and X. Jin, University of Manchester, UK

14.00 **EMBRACE: A Programmable Hardware Platform for Spiking Neural Networks** S. Hall (University of Liverpool), L. McDaid, J. Harkin (Ulster), P. Dudek (Manchester) and L. Smith(Sterling)

14.30 **Workshop breakout session** facilitated by partner organisations and aimed at identifying themes and research projects including those of use to industry

15.30 **Feedback session and discussion** – nominated speakers from each of the workgroups present the outcomes; followed by open discussion

16.00 Coffee

16.15 **Summary and follow-up** Daniel Dearing, eKTN

Networking and close

WS 6 Si-based Nanodevices for ultimate CMOS and beyond-CMOS

This workshop aims to establish a discussion forum in the field of nanoelectronics devices. It is supported by the SINANO Institute, which is a new European entity founded by the main laboratories of the European academic community working in this field, and by the European Network of Excellence NANOSIL devoted to Silicon-based Nanodevices funded by the European Commission for the 7th Framework Programme.

Over the next quarter-century, considerable challenges exist to push the limits of silicon integration down to nanometric dimensions and to enhance device performance in order to meet the ever increasing demands of communication and computing. The aim of the workshop is to present the status and trends of CMOS and beyond-CMOS nanodevices for terascale ICs.

9.00 **New Channel Materials for Ultimate CMOS** Siegfried Mantl, Institut für Bio- und Nanosysteme, Forschungszentrum Juelich

9.30 **Innovative Device Architectures Nanoscale CMOS** Nadine Collaert, IMEC

10.00 Refreshment break

10.30 **Comparative Analysis of Stress-Induced Performance Enhancement in NMOS and PMOS Transistors** David Esseni, Udine University

11.00 **Characterisation Methods for Nanodevices** Sorin Cristoloveanu, IMEP

11.30	**Emerging Nanotechnology for Integration of Nanostructures in Nanoelectronic Devices** Thierry Baron, LTM
12.00	Lunch
13.30	**Small Slope Switches** Adrian Ionescu, EPFL
14.00	**3D Multichannels and Stacked Nanowires Technologies** Thomas Ernst, LETI
14.30	**Carbon Nanotube – Silicon Heterojunctions for Nanoelectronics and Nanosensors** Jimmy Xu, Brown University
15.00	**Atomic Functionalities in Silicon Devices: Go Beyond the FET by Using Single Dopants and Artificial Silicon Atoms** Marc Sanquer, INAC
15.30	End of workshop

ESSCIRC fringe

The Edinburgh fringe will be held in the exhibition, which is situated n the Cromdale Hall. This session will take place during the afternoon coffee break on Tuesday 16 September 2008. Please refer to the timetable (p6) for further details. Presenters will also be on hand to discuss their posters outside this timeslot by prior arrangement. Please come to the registration desk to arrange an alternative session time.

P1 **Concept for a 12-bit Digital Bandpass Delta-Sigma Modulator for Power Amplifier Applications**
DipL-Ing Thomas Alpert, Universitat Stuttgart

P2 **On Current Reuse Shunt Feedback in 45 nm CMOS UWB RF Amplifier Design**
DipL-Ing S Hampel, Leibniz Universitat Hanover, Germany

P3 **A Real-Time K-means Learning Processor Architecture extendible to Multiple-Chip Large-Scale Systems**
Mr Yitao Ma, University of Tokyo, Japan

P4 **Two Stimulator Output Stages Isolated from DC Voltage Suitable for Safe Neuroprostheses**
Mr Xiao Liu, University College London, UK

P5 **A Digital Calibration Scheme for Low-Power A Digital Calibration Scheme for Low-Power Multi-Bit Pipeline ADCs**
Mr Tamin Faiq, University College London, UK

P6 **Low Power SRAM Cell Using Vertical Slit Field Effect Transistor (VeSFET)**
Mr Marcus Weis, Technische Universitat Munchen, Germany

P7 **Pipelined Inner Product Function Generator**
Mr Marco Castellano, University of Pavia, Italy

P8 **Spike-Based Methods for Programmable Analog Arrays Communication**
Mr Luiz Gouveia, University of Edinburgh, UK

P9 **100 nm Optical Resolution in Flip-Chip Integrated-Circuit Inspection**
Mr Keith Serrels, Heriot Watt University, UK

P10 **Automatic Synthesis of micro-Power and Compact Continuous Time Sigma-Delta for Probe Storage Device**
Mr José Bonan, University of Paris VI, Pierre & Marie Curie, France/IBM Research Laboratories, Switzerland

P11 **Variation Torelant Transceiver Design for System-on-Glass**
Mr Jinmyoung Kim, University of Tokyo, Japan

P12 **Interference Reduction Techniques in Neural Recording Tripoles: An Overview**

Mr Ioannis Pachnis, University College London, UK

P13 **Concept of Variable Capacitor based on Coulomb Blockade: A Top-Down Approach**
Mr Frederic Peschaud, Unite Mixte de Physique CNRS/Thales/ University Paris-Sud 11

P14 **CMOS-integrated Low-loss Porous Si Technology for on-chip RF Inductors**
Mr Filimon Zacharatos, IMEL/NCSR Demokritos, Greece

P15 **45 nm Ultra-Low Voltage Design**
Mr Fady Abouzeid, STMicroelectronics, France

P16 **A 0.35 im CMOS Continous Time Sigma Delta ADC Employing a PWM Time Encoding Technique**
Mr Ernesto Pun, Carlos III University, Spain

P17 **A Stereo Audio DAC with 97 dB Dynamic Range at 550 Microwatt Quiescent Power**
Mr Andrew Terry, Dialog Semiconductor

P18 **Synthesis of Asynchronous QDI FSM Based on Optimized Sequencers**
Mr Alsayeg Khaled, TIMA Laboratory, France

P19 **New Six Terminal Integrated Hall Element Model**
Mr Aleksander Sesek, University of Ljubljana, Slovenia

P20 **A Low-Voltage, Low-Power ADC for Body Sensor Interface**
Mr Alberto Rodríguez-Pérez, Institute of Microelectronics of Seville/University of Seville, Spain

P21 **Continuous-Time Bandpass Delta-Sigma Modulator with 8 GHz Sampling Frequency**
DipL-Ing Martin Schmidt, Universitat Stuttgart

P22 **Dual-Band TX-SAWless TD-HSDPA Chipset with Digital Interface for Baseband**
Dr Zhenbiao Li, Comlent Communications Inc, China

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