34th European Solid-State Circuits Conference
(ESSCIRC)
38th European Solid-State Device Research
Conference (ESSDERC)

15 September 2008
Edinburgh International Conference Centre,
Edinburgh – United Kingdom

PLL Design

The tutorial is aimed at engineers early in their careers who have a need to design a phase locked loop either as a part of a university research project, or as a design project within industry. The course will assume a first degree level working knowledge of electronic engineering. It will introduce the phase locked loop and the general theory of the loop, and then progress to give practical implementations of all the components of the loop for a variety of different applications.

1. The Pll loop:
Carlo Samori, Politecnico di Milano, Italy

Topics:

- The PLL loop as a phase feedback system
- Analysis of the loop. Type I and type II definition
- Charge pump PLL
- Phase/frequency detection
- Discrete time effects the Gardner's limit to bandwidth
- Noise in the loop – relationship between noise and Jitter.
- Spurs in PLL
- Components of the loop, how their performance influences the overall loop

2. Example – The Radio Synthesiser
Carlo Samori, Politecnico di Milano, Italy

Topics:

- Offset PLL
- The fractional n- divider, fractional spurs
- Sigma delta control of the division ratio
- Examples of practical realisations

3. Example – Clock recovery from a pseudo random bit stream
Ivan Bietti, ST Microelectronics

4. Example – Digital pll for clock generation
Jan-Peter Frambach, NXP Nijmegen, The Netherlands

Topics:

- Analogue vs Digital PLL; the essential differences
  - Is an analogue PLL really a PLL
  - DPLL; a true phase domain loop
- Type of DPLL's
  - True phase domain PLL
  - Bang-bang PLL
- DPLL Building blocks
  - Time-to-Digital converter
  - Phase Detector

- Narrow Band / Wide Band DPLL

5. Questions and answer session

Programme Timings

13.30-15.00 The Pll Loop, Carlo Samori, Politecnico di Milano, Italy

15.30-16.00 Example 1 – The Radio Synthesiser, Carlo Samori, Politecnico di Milano, Italy

16.00-16.30 Example 2 – Clock Recovery from a Pseudo Random Bit Stream, Ivan Bietti, ST Microelectronics, Crolles, France

16.30-17.00 Example 3 – Digitial Pll for Clock Generation, Jan-Peter Frambach, NXP Nijmegen, The Netherlands

17.00-17.15 Question and Answer Session

Biographies:

Carlo Samori – Received the PhD in Electrical Engineer and Communication from the Politecnico di Milano, where he is now an Associate Professor. His main research interests are in the field of low-phase noise VCO and PLL architectures.

Jan Peter Frambach - received the M.Sc. degree from Delft University of Technology (TUD), The Netherlands, in 1994. He joined Philips Semiconductors in 1995. He has worked on Optical Networking BiCMOS chipsets up to 10Gbit/s; Wideband Amplifiers, Data & Clock Recovery, High Speed (De)Serializers, Cross Point Switches. Since 2003 he has been developing wireless integrated transceivers in RF-CMOS. His current research interests are: Oscillators (RF and LF), PLL's, Data Converters and PA's. Currently he is leading the Bluetooth 45nm Transceiver development team at NXP Semiconductors