ESSDERC ESSCIRC 2008
34th European Solid-State Circuits Conference (ESSCIRC)
38th European Solid-State Device Research Conference (ESSDERC)
19 September 2008
Edinburgh International Conference Centre, Edinburgh – United Kingdom

Workshop on Germanium and III-V MOS Technology

The time when technology-driven dimensional scaling could provide simultaneously high-density/low cost and high performance circuits is over. Further scaling does not guarantee performance benefits. From now on, novel device architectures and new materials may be necessary to obtain the required performance. In fact, Hf-based dielectric/metal gate combinations have replaced the long standing SiO_2/polysilicon in the gate of transistors. The new gates are already in production for the 45 nm CMOS since the end of 2007 by leading ICs manufacturer. What is next? Some people believe that new high mobility channels such as germanium and III-V compounds may be needed for future device generations.

In this workshop experts from academia, technology development laboratories and semiconductor manufacturers will come together to discuss the challenges toward a viable high mobility MOS technology. The experts will describe large scale initiatives in the US, Asia and Europe and they will introduce the main issues which will be subsequently debated in two panel discussions.

In the first morning session we will address issues related to gate dielectric and device architecture and performance. At the end, during the panel discussion we will try to answer a few difficult questions. Is it feasible to develop a complementary MOS technology which will be based entirely on Germanium? The answer to this question is not easy at the present time. We can only say that Ge CMOS is highly desirable because it simplifies processing. The main obstacle is that Ge nMOSFETs do not work as expected and we do not know why. Is this problem related to materials and/or device processing or is it of more fundamental nature related to the semiconductor itself? In the case of III-V MOSFETs, the problems are even more difficult to solve. The consensus is that a high density of defect states, probably near midgap, pin the Fermi level, thus inhibiting inversion in GaAs. Which is the best way to passivate the GaAs surface? Which is the best device architecture and operation mode? Is it better to go for surface inversion-type with implanted S/D or buried channel implant-free devices? Is InGaAs channel better than GaAs and why?

While high mobility channels show advantage over Si in discrete long channel research devices, the situation becomes unclear when dimensions shrink. Will mobility retain high values or will it degrade as in the case of Si nanoscaled devices? More importantly, is mobility a relevant physical quantity at nanoscale dimensions or perhaps quasi-ballistic transport sets new rules for the on-state current and performance in general? Will the off-state current be under control especially for Ge devices which are expected to suffer from band-to-band tunneling?

During the second session in the afternoon and in the panel discussion at the end we will address integration issues including heteroepitaxy and engineered substrates, self-aligned processing, junctions and contacts. As it looks right now, Ge performs well for pMOS only while III-V compounds are good for nMOS, therefore Ge and III-V compounds are not competing materials; rather, they could complement each other to form a dual-channel CMOS, provided that a good co-integration scheme can be found. Which will be the best starting substrate, plain Si or GeOI? Do we have good solutions for the problems associated with heteroepitaxial growth of III-V compounds on Ge or Si? Is dual-channel Ge/III-V better than Ge/s-Si counterpart? Do we know how to process III-Vs in a self-aligned way to guarantee scaling to very small dimensions? After all, is high mobility dual-channel CMOS scalable and manufacturable so that it could be a viable technology for volume production?

The workshop is sponsored by the European FP7-ICT project DUALLOGIC-"*Dual channel CMOS for (sub)-22 nm high performance logic*" http://www.ims.demokritos.gr/DUALLOGIC

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Organizer : A. Dimoulas, NCSR DEMOKRITOS

Program

Session 1: Gate materials and devices

9:00	D. Antoniadis	MIT	Overview of advanced high mobility/high velocity research devices
9:20	M. Rodwell	UCSB	Device architecture and processing for III-V MOS technology
9:40	S. Takagi	University of Tokyo	Devices for high performance CMOS
10:00	Coffee break		
10:20	T. Krishnamohan	Intel/Stanford U.	Nanoscale Ge and III-V FETs
10:40	M. Hong	Nat. Tsing Hua U.	GaGdO and Al_2O_3- passivated III-V MOSFETs
11:00	J. Fompeyrine	IBM-Zurich Res. Lab.	*a* -Si-passivated III-V MOSFETs
11:20	**Panel discussion 1**	Speakers session 1, moderator A. Dimoulas	
12:00	Lunch		

Session 2: Substrates and Integration

13:30	T. Skotnicki	ST Microelectronics	Ge-on-Nothing for ultrathin Ge film integration
13:50	L. Clavelier	CEA-LETI	GeOI/sSOI for co-inegration of s-Ge pMOS with s-Si nMOS
14:10	M. Heyns	IMEC	Sub-100 nm Ge pMOS using Si-compatible process flow
14:30	R. Jammy	SEMATECH	Co-integration of Ge pMOS with III-V nMOS for heterogeneous CMOS
14:50	I. Thayne	U. Glasgow	Process modules for implant-free III-V MOSFETs
15:10	**Panel discussion 2**	Speakers session 2, moderator A. Dimoulas	
15:50	End		

Registration

To register for this workshop, please complete the on-line registration form found in this address:
http://members.iop.org/eventbooking.asp?mastereventcode=CE&eventcode=7891
Please note that the workshop will be free of charge and it includes admission, coffee break and lunch.
The registration deadline is 5 September 2009.