34th European Solid-State Circuits Conference
(ESSCIRC)
38th European Solid-State Device Research
Conference (ESSDERC)

15 September 2008
Edinburgh International Conference Centre,
Edinburgh – United Kingdom

Filter Design

The tutorial is aimed at engineers early in their careers who have a need to design integrated filters either as a part of a university research project, or as a design project within industry. The course will assume a first degree level working knowledge of electronic engineering. It will refresh basic filter theory, and then progress to give practical implementations of both analogue and digital filters.

1. Filter Theory

Bram Nauta, Professor of Electrical Engineering at the University of Twenty, The Netherlands.

Topics:

-Amplitude and group delay responses of standard filter forms

Filter synthesis; from mathematical formula to circuit representation

Non-idealities in filters (noise, distortion, phase error); improvements through filter topology choice

Practical comments on implementation of building blocks

2. Tuning and reconfiguration for analog filters:

Andreia Cathelin, ST Microelectronics, Crolles, France

Topics:

Influence of process, voltage and temperature variations on filter behavior
Tuning/trimming methodology: direct, indirect methods
- Implementation theory: on the use of the Master-Slave technique (PLL, ALL, etc…)
- Physical implementation examples on Gm-C filter circuits for mobile communications applications in zero-IF architecture

System need for reconfigurable filter architectures
Reconfigurable filter concept: work methodology

3. Discrete Time including digital filters

Markus Helfenstein, NXP, Zurich, Switzerland

Topics:

An introduction to discrete time signals:
- Basic z- transform properties
- Time to frequency domain transformation
- The need for anti-aliasing/ reconstruction filters.

Discrete time, Analog filters - a brief overview of switched-cap filters

Design techniques for digital filters

Examples: Two examples will be ‘walked through’ to illustrate the above techniques

4. Question and Answer Session

Programme Times:

Agenda:

08.30-09.45 Filter Theory, Bram Nauta, University of Twente, The Netherlands

10.00-10.45 Tuning and Reconfiguration for Analog Filters, Andreia Cathelin, ST Microelectronics, Crolles, France

11.00-12.15 Discrete Time Including Digital Filters, Markus Helfenstein, NXP, Zurich, Switzerland

12.15-12.30 Question and Answer Session

Biographies:

Bram Nauta received the M.Sc degree (cum laude) in electrical engineering from the University of Twente, Enschede, The Netherlands, and his Ph.D. degree from the same university on the subject of analog CMOS filters for very high frequencies.
In 1991 he joined Philips Research, where he worked on high speed AD converters and analog key modules. In 1998 he returned to the University of Twente, as full professor heading the IC Design group. His current research interest is high-speed analog CMOS circuits.
He is Editor-in-Chief for the IEEE Journal of Solid-State Circuits. He is also member of the technical program committees of the International Solid State Circuits Conference (ISSCC), the European Solid State Circuit Conference (ESSCIRC), and the Symposium on VLSI circuits. He is co-recipient of the ISSCC 2002 "Van Vessem Outstanding Paper Award", is distinguished lecturer of the IEEE, elected member of IEEE-SSCS AdCom and is IEEE fellow.

Markus Helfenstein received the Bachelor degree from the Inst. of Technology in Lucerne in 1986, the diploma and the Dr. Sc. Techn. degree in electrical engineering from the Swiss Federal Institute of Technology in 1992 and 1997. In 2007 he also earned an executive MBA from the University of Fribourg, Switzerland.

From 1986 to 1988 he was with Mettler Instrumente AG, Switzerland, involved in the design of high resolution counter IC chips. Between 1996 and 1998 he was a lecturer for digital signal processing at the Inst. of Technology in Lucerne. In 1998, he co-founded Anadec GmbH, a start-up company which holds patents on the design of analog VLSI iterative decoders. Between 2000 and 2002 he was with Globespan Inc. (now Conexant) involved in projects on the design of mixed-signal chips for xDSL applications. He joined the Cellular Systems team of Philips (now NXP) in 2002. He is now a development manager at NXP and involved in projects utilising GSM/EDGE/UMTS mixed-signal chips.

He is a past associate editor of the Transactions on Circuits and Systems (TCAS-II) and he is member of the technical program committee of the European Solid State Circuit Conference (ESSCIRC).

Andreia Cathelin started her electronic studies at the Polytechnic Institute of Bucarest, Romania and graduated from the Institut Supérieur d’Electronique du Nord (ISEN), Lille, France in 1994. From 1994 till 1998, she prepared a Ph. D. thesis with IEMN/ISEN, Lille, France and MS2 Company, Roubaix, France on a fully-integrated BiCMOS low power – low voltage FM/RDS receiver.
From 1997 till 1998, she was with Info Technologies, Gradignan, France, working on analog and RF communications design. Since 1998, she is with ST Microelectronics,

Crolles, France, now in the Technology R&D, Central CAD and Design Solutions, CMOS System Architecture RF design team in Minatec, Grenoble.
She is a senior design expert and her major fields of interest are RF and mmW systems for wireless communications, MEMS devices co-integration and SOI technologies.