# CMOS at the Bleeding Edge

This tutorial will describe state of the art CMOS from both an industrial and academic perspective. Internationally leading experts will give authoritative presentations of the current status, future directions and challenges facing advanced silicon technology. The tutorial will appeal to graduate students and young engineers who want to gain a broader perspective of the field as well as to more experienced engineers and managers.

8.30 Introduction
*A O'Neill (Newcastle University, UK)*

8.40 CMOS scaling into the next decade: An industrial perspective of challenges and opportunities
*P Mahji (Intel/Sematech, USA)*

9.20 High mobility channel MOSFET
*S Takagi (Tokyo University, Japan)*

10.00 Future gate stack materials
*O Engstrom (Chalmers University, Sweden)*

10.40 Coffee

11.00 Variability
*A Asenov (Glasgow University)*

11.40 The SOI Mosfet: from single gate to multigate
*J-P Colinge (Tyndall National Institute, Ireland)*

12.20 Close

**Biographies of speakers**

**Anthony O'Neill** was born in Leicester, England in 1959. He received the BSc degree from the University of Nottingham in 1980 and the PhD degree from the University of St Andrews three years later. Between 1983 and 1986 he worked for Plessey Research (Caswell) Ltd before taking up his post at the University of Newcastle upon Tyne. He has worked on a wide range of topics in the field of semiconductor device and process technology and published many papers. IN 1994 he was Visiting Scientist at MIT (Microsystems Technology Laboratories) and in 2002 he became a Royal Society Industry Fellow with Amtel. He was appointed to a personal chair in physical electronics and since 1996 has been Siemans Professor of Microelectronics. He is an IEEE Distinguished Lecturer, a Fellow of the IET and a director of the National Microelectronics Institute, UK. Current research interests include Si, strained Si/SiGe and SiC device and process technologies and interconnect reliability. He is the chair for tutorials and workshops at ESSDERC 2008.

**Prashant Majhi** received his Bachelors of Technology degree from the Indian Institute of Technology, Madras (1996), and his Ph.D. degree in science and engineering of materials program

from Arizona State University, Tempe, AZ (2000). He joined Phillips Semiconductor in The Netherlands and worked on several CMOS and mixed-signal process technologies. In 2004, he joined Intel Corp., and is currently at SEMATECH as an Intel Assignee managing the CMOS scaling group.

**Shin-ichi Takagi** was born in Tokyo, Japan, on August 25, 1959. He received the B.S., M.S. and Ph.D. degrees in electronic engineering from the University of Tokyo, Tokyo, Japan, in 1982, 1984 and 1987, respectively. His Ph.D. thesis involved the study on the surface carrier transport in MISFETs based on III-V semiconductors. He joined the Toshiba Research and Development Center, Kawasaki, Japan, in 1987, where he has been engaged in the research on the device physics of Si MOSFETs, including the carrier transport in the inversion layer, the impact ionization phenomena, the hot carrier degradation and the electric properties of Si/ $SiO_2$ interface. From 1993 to 1995, he was a Visiting Scholar at Stanford University, Stanford, CA, where he studied the Si/SiGe hetero-structure devices. Since returning to the ULSI Research Laboratories, he was also engaged in the physics and technology of the reliability of $SiO_2$, ferroelectric devices and strained-Si MOS devices. From 2001 to 2008, he worked for the MIRAI Project, as the leader of Ultra-High Performance New Transistor Structures Theme. In October 2003, he moved to the University of Tokyo, where he is currently working as a professor in the department of Electronic Engineering, School of Engineering. His recent interests include the science and the technologies of advanced Si CMOS and high performance CMOS devices using new channel materials such as strained-Si, Ge and III-Vs. Dr. Takagi served on the technical program committee on several international conferences including International Electron Device Meeting, International Reliability Physics Symposium, International Conference on Solid State Device and Materials and International Solid State Circuits Conference. He is a member of the IEEE Electron Device Society and the Japan Society of Applied Physics.

**Olof Engström** received a PhD degree in Solid State Physics from the University of Lund in 1975 and was later employed by ASEA AB for research on high power thyristors, by AB Rifa for development of MOS technology and by the Swedish Defence Research Institute for sensor research. In 1984, he came to Chalmers University of Technology as a professor in Solid State Electronics. Between 1996 and 1999, he served as Dean of Chalmers School of Electrical and Computer Engineering and 1999 - 2002 he was the Director of the Microtechnology Center at Chalmers (MC2). From 2003 he is back in research as a professor at the Department of Microtechnology and Nanoscience of MC2. His present research interest is in, high-k-materials and semiconductor quantum structures. In 1991, he founded Samba Sensors AB, a company for production of fiberoptical pressure sensors. He is a member of the Royal Swedish Academy of Engineering Science, the Finnish Society of Science and the High-k-Gang (www.high-k-gang.eu)..

**Asen Asenov** received his MSc degree in solid state physics from Sofia University, Bulgaria in 1979 and the PhD degree in physics from The Bulgarian Academy of Science in 1989. He is a professor of Device Modelling, Leader of the Glasgow Device Modelling Group and Academic Director of the Glasgow Process and Device Simulation Centre he coordinates the development of 2D and 3D quantum mechanical, Monte Carlo and classical device simulators and their application in the design of advanced and novel CMOS devices. He has pioneered the simulations of statistical variability in nano-CMOS devices including random dopants, interface roughness and line edge roughness. He has over 450 publications in the above areas.

**Jean-Pierre Colinge** received a BS degree in Philosophy, the Electrical Engineer degree, and the Ph.D. degree in Applied Sciences from the Université Catholique de Louvain, Louvain-la-Neuve, Belgium, in 1980, 1980, and 1984, respectively. He worked at the Centre National d'Etudes des Télécommunications (CNET), Meylan, France, at the Hewlett-Packard Laboratories, Palo Alto, USA, at IMEC, Leuven, Belgium, where he was involved in SOI technology for VLSI and special device applications. From 1991 to 1997, Dr. Colinge was professor at the Université catholique de Louvain, leading a research team in the field of SOI technology for low-power, radiation-hard, high-temperature and RF applications as well as reduced-dimension devices (thin double-gate and quantum-wire MOSFETs). From 1997 to 2006 he was professor at the University of California at Davis, carrying on research on advanced multi-gate SOI MOS devices. He has been on the committee of several conferences, including IEDM and SSDM, has been General Chairman of the

IEEE SOS/SOI Technology Conference in 1988, and is a Fellow of IEEE. He has published over 300 scientific papers and four books on the field of SOI as well as two books on semiconductor device physics. Prof. Colinge is currently Professor at the Tyndall National Institute, Ireland, where he is working on the modeling, fabrication and characterization of advanced SOI MOS devices.