34th European Solid-State Circuits Conference
(ESSCIRC)
38th European Solid-State Device Research
Conference (ESSDERC)

15 September 2008
Edinburgh International Conference Centre,
Edinburgh – United Kingdom

All you want to know about RF CMOS – 1 GHz to 0.01THz

The short course is aimed at making practising engineers aware of the rapid advances that are occurring in RFCMOS as the line widths reduce below 90nm. This has pushed the upper frequency capability towards 0.1THz. With this move up in frequency, there is a necessity to refine measurement techniques to get signals on and off the chip, to improve modelling of device behaviour, improve modelling of passive structures to guide the signal on the chip and to select architectures that lend themselves to CMOS implementation. In this course experts will present these skills which are essential for design new frequency limits and will improve understanding at lower frequencies.

1. Making measurements on chip at 50 -100 GHz.
Mikko Kantanen, MilliLab, Finland

Topics

- On-wafer s-parameter, linearity, noise figure, and noise parameter measurement techniques up to 110 GHz.
- On-wafer interface: Signal routing using waveguides or thin coax cables, requirements to circuit design to make measurements easier.
- Most common on-wafer calibration techniques for mm wave s-parameter measurements.
- Typical measurement setups with practical considerations are described using examples.

2. Construction, modelling and characterisation of passives on silicon for RF and millimetre-wave applications
John R Long, Electronics Research Laboratory/DIMES, Delft University of Technology, The Netherlands

Topics:

- Modeling, simulation, physical layout and design of monolithic passive elements for RF and high-speed applications.
- Circuit models for RLC components, interconnect wiring (including microstrip and coplanar waveguide) and other distributed parameter passive elements, such as transformers and transformer baluns.
- Simulation of passive components with traditional IC simulation tools such as SPICE and other RF simulators (e.g., Agilent-ADS).
- The limitations and advantages of on-chip passives to the circuit designer at microwave and millimetre-wave frequencies are described using case studies from transceiver applications.

3. RF Modelling of MOS transistors for 0.1THz operation
Christian Enz, Professor Electronic Engineering, EPFL, Switzerland

Topics:

- From threshold-based models to charge & surface potential models (PSP, BSIM4, EKV)
- The static charge-based model including DIBL, gate current, mobility reduction, velocity saturation
- What changes at RF? Including non-quasi-static operation and RF figures of merit
- Small-signal charge-based model, inlcuding gate resistance and substrate network.
- Noise Model

4. RF Circuits for UWB, 3GHz to 10GHz
Domine Leenaerts NXP, Eindhoven, The Netherlands

Topics:

- Presentation of designs of LNA, frequency divider and full receiver chain for UWB
- Comparison of circuit performance over process nodes (90nm, 65nm and 45nm).
- Comparison of RF measures (ft, ftmax ,NFmin) over the same process nodes Including real effects of device connections.

5. Design of amplifiers and mixers in baseline CMOS technology
Mikko Varonen, Helsinki University of Technology, Finland

Topics:

- The design flow and methodology of millimeter-wave integrated circuits in baseline CMOS technology are discussed.
- The simulation and measurement results of active and passive test structures such as transistors, coplanar waveguides, capacitors and a spiral transmission line balun are presented.
- The design of millimeter-wave CMOS amplifiers are discussed.
- The design of millimeter-wave up and down conversion mixer circuits are discussed.
- Measurement results of implemented CMOS amplifiers and mixers are presented.

6. Millimeter wave design in bulk and SOI CMOS
Andreia Cathelin, ST Microelectronics, Crolles, France

Topics:

- Target applications for the Millimeter-wave frequency band
- Silicon technologies to address mmW complete solutions
- Active devices on bulk and SOI technologies
- LNA mmW designs Down-conversion mixers for mmW
- Voltage controlled oscillators for mmW
- Power amplifiers for mmW
- Conclusions

7. RF Assembly and Packaging – Ongoing system integration
Klaus Pressel, Infineon Technologies, Regensburg, Germany

Topics:

- Overview on basic package technologies including : flip chip and wire bonding and their RF capabilities is given.
- Technologies considered include thinning, dicing, shielding, heat dissipation, and stacking into the 3rd dimension. The impact of warpage, especially for system-in-package, is considered.

- An innovative assembly and interconnect solution based on wafer level packaging allowing improved RF performance - also for ≤ 65nm technologies - both for SoC and SiP is presented.
- Choices to integrate passive components are discussed.
- The impact to consider also the package/board interface is taken into account.
- We show examples for CMOS devices and for SiGe based devices with frequencies up to the mm-wave range (about 80 GHz).
- The importance of coherent chip/package/board co-design is highlighted. All these developments require the involvement of chip and assembly & package design teams from the very beginning of product design.

8. RF Radio Architectures/system design for CMOS applications
Hooman Darabi. Broadcom Irvine California, USA

Topics:

- General system level concerns for CMOS transceivers are described: eg linearity, frequency planning, blockers spurious mixing
- Various radio architectures suitable for different standards such as cellular, Bluetooth, and WLAN are presented, and the trade-offs are discussed.

9. Question and answer session

Programme Timings

09.00-09.50 Making Measurements on Chip at 50-100GHz, Mikko Kantanen, MilliLab, Finland

09.50-10.40 Construction, Modelling and Characterisation of Passives on Silicon for RF and Millimetre-Wave Applications, John R. Long, Electronics Research Laboratory/DIMES, Delft University of Technology, The Netherlands

11.00-11.50 RF Modelling of MOS Transistors for 0.1THz Operation, Christian Enz, EPFL, Switzerland

11.50-12.20 RF Circuits for UWB, 3GHz to 10GHz, Domine Leenaerts, NXP, Eindhoven

12.20-13.30 Lunch

13.30-14.00 Design of Amplifiers and Mixers in Baseline CMOS Technology, Mikko Varonen, Helsinki University of Technology

14.00-14.30 Millimeter Wave Design in Bulk and SOI CMOS, Andreia Cathelin, ST Microelectronics, Crolles, France

14.30-15.20 RF Assembly and Packaging – Ongoing System Integration, Klaus Pressel, Infineon Technologies, Regensburg, Germany

15.45-16.35 RF Radio Architectures/System Design for CMOS Applications, Hooman Darabi, Broadcom Irvine, California, USA

16.35-16.50 Question and Answer Session

Biographies

Mikko Kantanen received his Master of Science (Tech.) and Licentiate of Science (Tech.) degrees in Electrical Engineering from Helsinki University of Technology (TKK), Espoo, Finland 2001 and 2006, respectively. He is currently working towards the Ph.D. degree.
Since 2001 he has worked as a Research Scientist in MilliLab, VTT Technical Research Centre of Finland, Espoo, Finland, in the areas of millimeter wave integrated circuit design, millimeter wave measurements, and millimeter wave systems.
Mr. Kantanen is a recipient of an Asia-Pacific Microwave Conference 2006 Prize.

John Long received the M.Eng. and Ph.D. degrees in Electronics from Carleton University in 1992 and 1996, respectively. He worked for 12 years at Bell-Northern Research on Gbit/s fiber systems, and for 5 years at the University of Toronto. In 2002, he joined the Delft University of Technology as Chair of the Electronics Research Laboratory. His current research interests include: mm-wave IC design, low-power transceiver circuitry for broadband and highly-integrated radios, and electronics for high-speed datacomm systems.

Christian Enz (M'84) received the M.S. and Ph.D. degrees in electrical engineering from the Swiss Federal Institute of Technology, Lausanne (EPFL) in 1984 and 1989 respectively. From 1984 to 1989 he was research assistant at the EPFL, working in the field of micropower analog CMOS integrated circuits (IC) design. In 1989 he was one of the founders of Smart Silicon Systems S.A. (S3), where he developed several low-noise and low-power ICs, mainly for high energy physics applications. From 1992 to 1997, he was an Assistant Professor at EPFL, working in the field of low-power analog CMOS and BiCMOS IC design and device modeling. From 1997 to 1999, he was Principal Senior Engineer at Conexant (formerly Rockwell Semiconductor Systems), Newport Beach, CA, where he was responsible for the modeling and characterization of MOS transistors for the design of RF CMOS circuits. In 1999, he joined the Swiss Center for Electronics and Microtechnology (CSEM) where he launched and lead the RF and Analog IC design group. In 2000, he was promoted Vice President, heading the Microelectronics Department. He is also lecturing and supervising undergraduate and graduate students in the field of analog and RF IC design at EPFL, where he is Professor since 1999. His technical interests and expertise are in the field of very low-power analog and RF IC design and semiconductor device modeling, with a particular focus on noise. He is the author and co-author of more than 140 scientific papers and has contributed to numerous conference presentations and advanced engineering courses. Together with E. Vittoz and F. Krummenacher he is one of the developer of the EKV MOS transistor model and the author of the book "Charge-Based MOS Transistor Modeling - The EKV Model for Low-Power and RF IC Design" (Wiley, 2006). He is member of several technical program committees, including International Solid-State Circuits Conference (ISSCC) and European Solid-State Circuits Conference (ESSCIRC). He has served as a vice-chair for the 2000 International Symposium on Low Power Electronics and Design (ISLPED), exhibit chair for the 2000 International Symposium on Circuits and Systems (ISCAS) and is chair of the technical program committee for the 2006 European Solid-State Circuits Conference (ESSCIRC).
He is a member of IEEE and Chair of the IEEE Solid-State Chapter of West Switzerland.

Domine M. W. Leenaerts (M'94-SM'96-F'2005) received the Ph.D. degree in electrical engineering from Eindhoven University of Technology, Eindhoven, the Netherlands, in 1992. From 1992 to 1999, he was with Eindhoven University of Technology as an Associate Professor with the Micro-electronic Circuit Design group. In 1995, he was a Visiting Scholar with the Department of Electrical Engineering and Computer Science, University of California, Berkeley. In 1997, he was an Invited Professor with the Technical University of Lausanne (EPFL), Lausanne, Switzerland. From 1999 until 2006, he has been with Philips Research Laboratories. Since 2007 he is with NXP Semiconductors, Research as senior principal scientist, involved in RF integrated transceiver design. He has published over 150 papers in scientific and technical journals and conference proceedings and holds over 20 US patents. He has coauthored several books, including *Circuit Design for RF Transceivers* (Boston, MA: Kluwer, 2001). Dr. Leenaerts served as IEEE Distinguished Lecturer in 2001-2003 and served as Associate Editor of the IEEE Transactions on Circuits and Systems-Part I (2002-2004). Since 2005 he is the IEEE Circuits and Systems Society Member representative in the IEEE Solid-State Circuits Society Administrative

Committee. Since 2007 he serves as Associate Editor of the IEEE Journal of Solid-State Circuits. He is member of the technical program committees of ISSCC, ESSCIRC, and RFIC.

Andreia Cathelin, started her electronic studies at the Polytechnic Institute of Bucarest, Romania and graduated from the Institut Supérieur d'Electronique du Nord (ISEN), Lille, France in 1994. From 1994 till 1998, she prepared a Ph. D. thesis with IEMN/ISEN, Lille, France and MS2 Company, Roubaix, France on a fully-integrated BiCMOS low power – low voltage FM/RDS receiver.
From 1997 till 1998, she was with Info Technologies, Gradignan, France, working on analog and RF communications design. Since 1998, she is with ST Microelectronics, Crolles, France, now in the Technology R&D, Central CAD and Design Solutions, CMOS System Architecture RF design team in Minatec, Grenoble.
She is a senior design expert and her major fields of interest are RF and mmW systems for wireless communications, MEMS devices co-integration and SOI technologies.

Klaus Pressel received his PhD from the University of Stuttgart on investigations of point defects in III/V semiconductor devices. He worked for 8 years at the IHP Frankfurt (Oder) on both Si CMOS and SiGe:C research and technology. He was a department head for „Material, Diagnostics, Foundry", and strongly supported the set-up of analogue and digital circuit design capability. With his team Klaus was responsible for characterization of IHP's SiGe:C BiCMOS technology, reliability, testing, SPICE parameter extraction etc. In 2001 Klaus joined Infineon Technologies, where he focuses now on innovations in assembly and interconnect technology. His special interests are System-in-Package solutions and high frequency applications. Klaus is representing Infineon in the European MEDEA+/CATRENE steering group technology, EURIPIDES technical committee, ITRS, and JISSO. He has a long term experience in European and German funded research projects to look into future technologies. He is author/co-author of more than 100 papers/publications in semiconductor physics and technology, circuit design, assembly and interconnect technologies.

Hooman Darabi received the Ph.D. degree in electrical engineering from the University of California, Los Angeles in 1999. He is currently a director, engineering, with Broadcom Corporation, Irvine, CA. His interests include analog and RF IC design for wireless communications, including Bluetooth, WLAN, and cellular applications.